Power-Efficient Breadth-First Search with DRAM Row Buffer Locality-Aware Address Mapping

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HPGDMP ’16, Salt Lake City, November 13, 2016

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  - Social networking services
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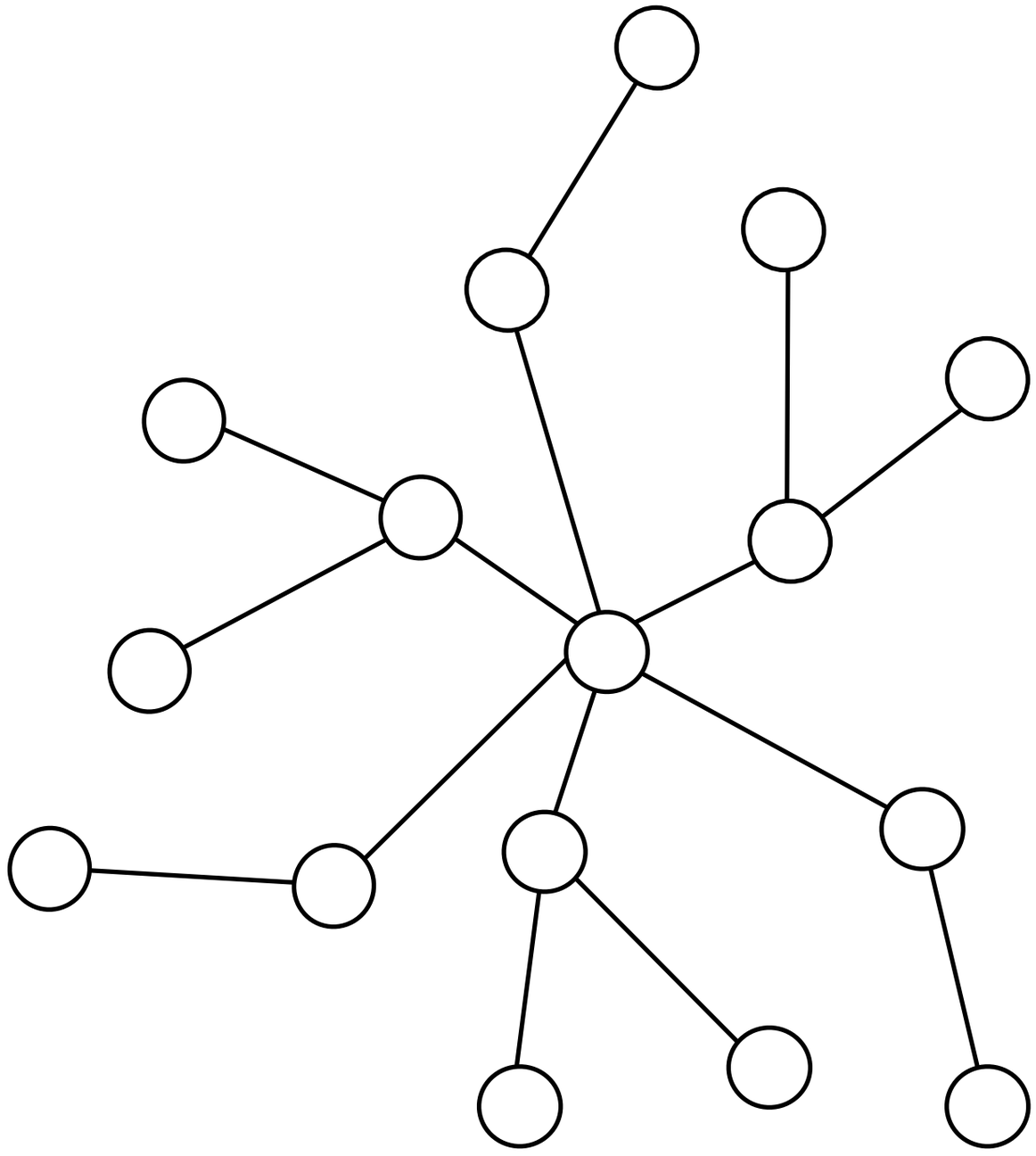

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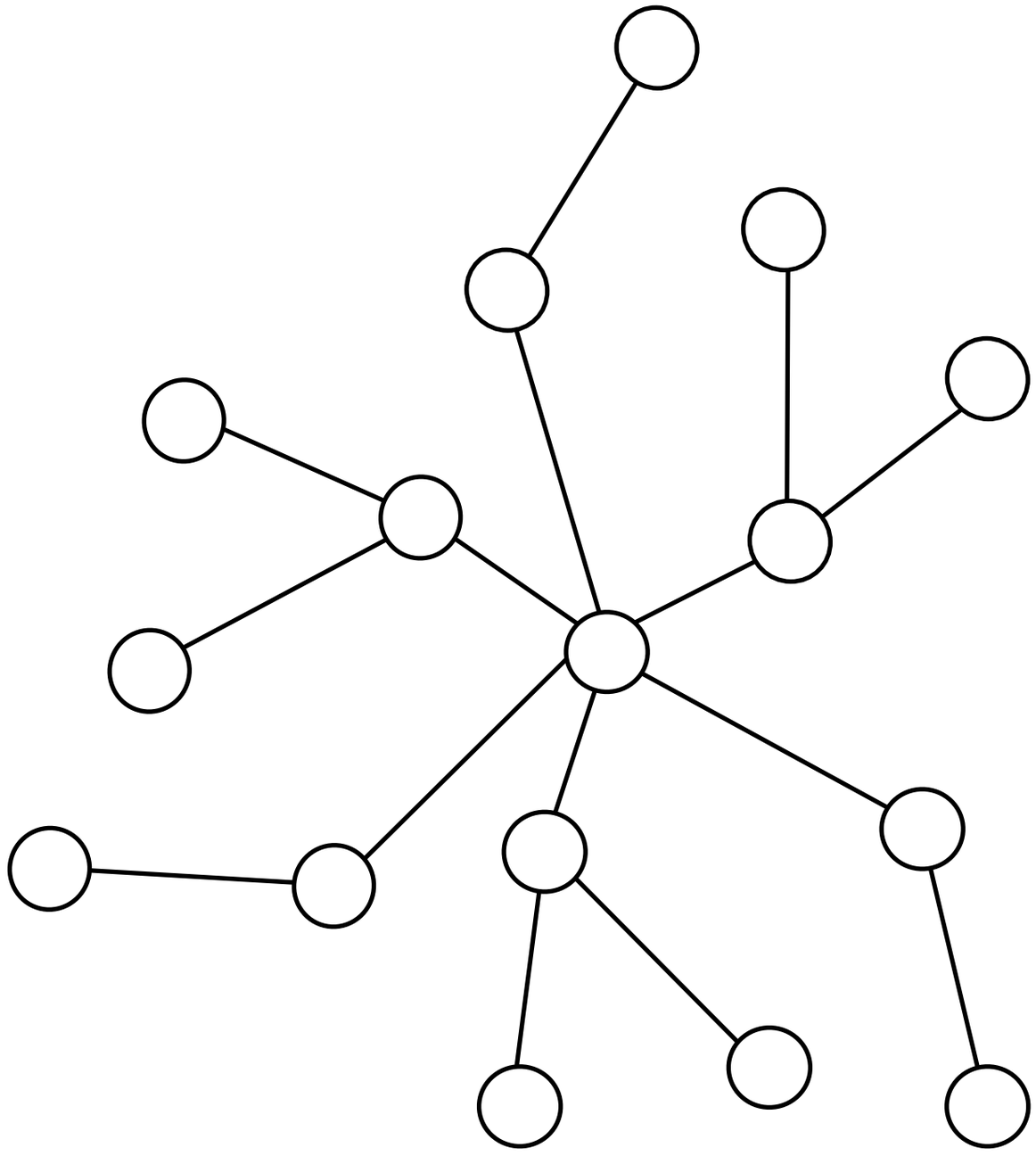

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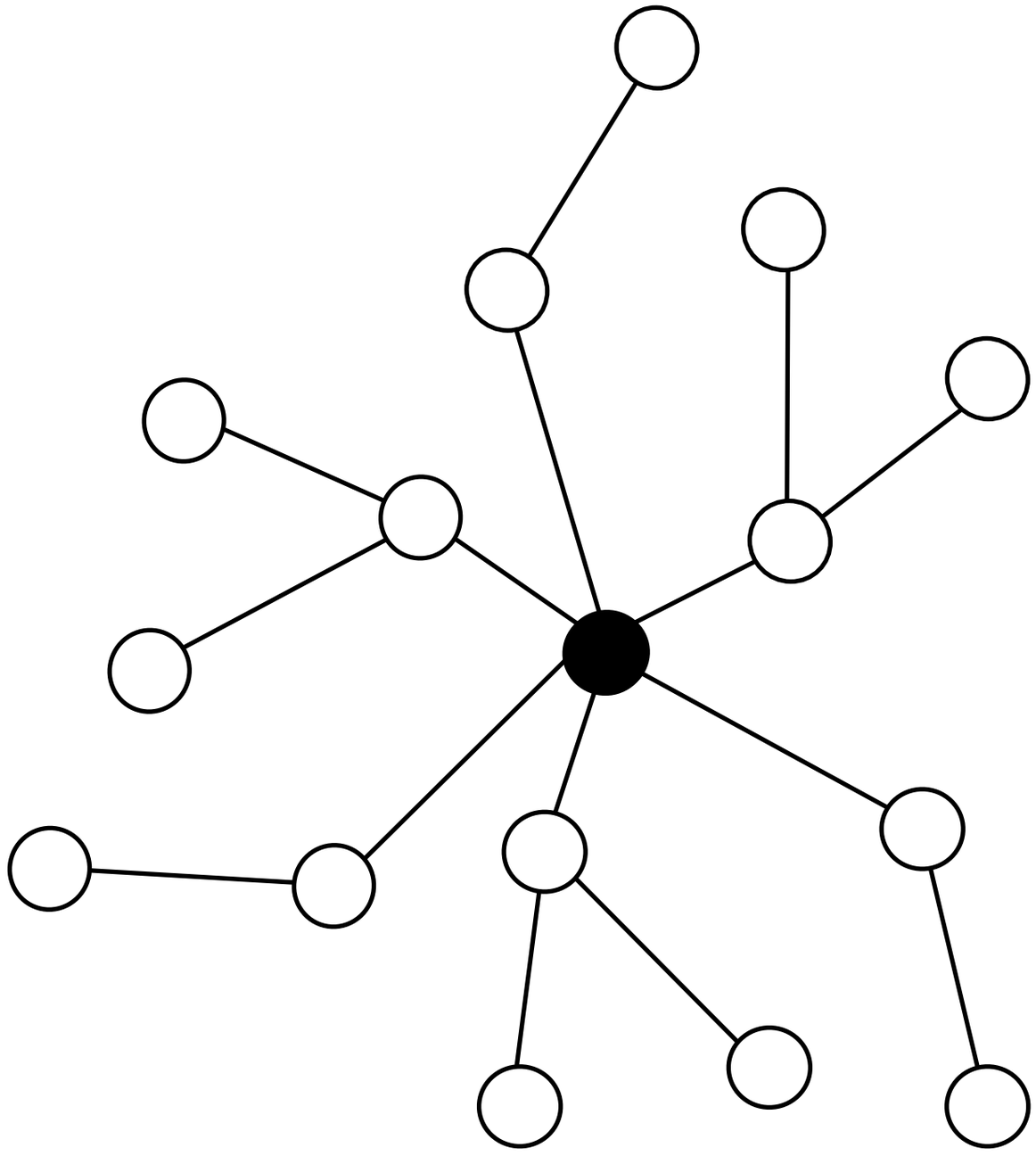

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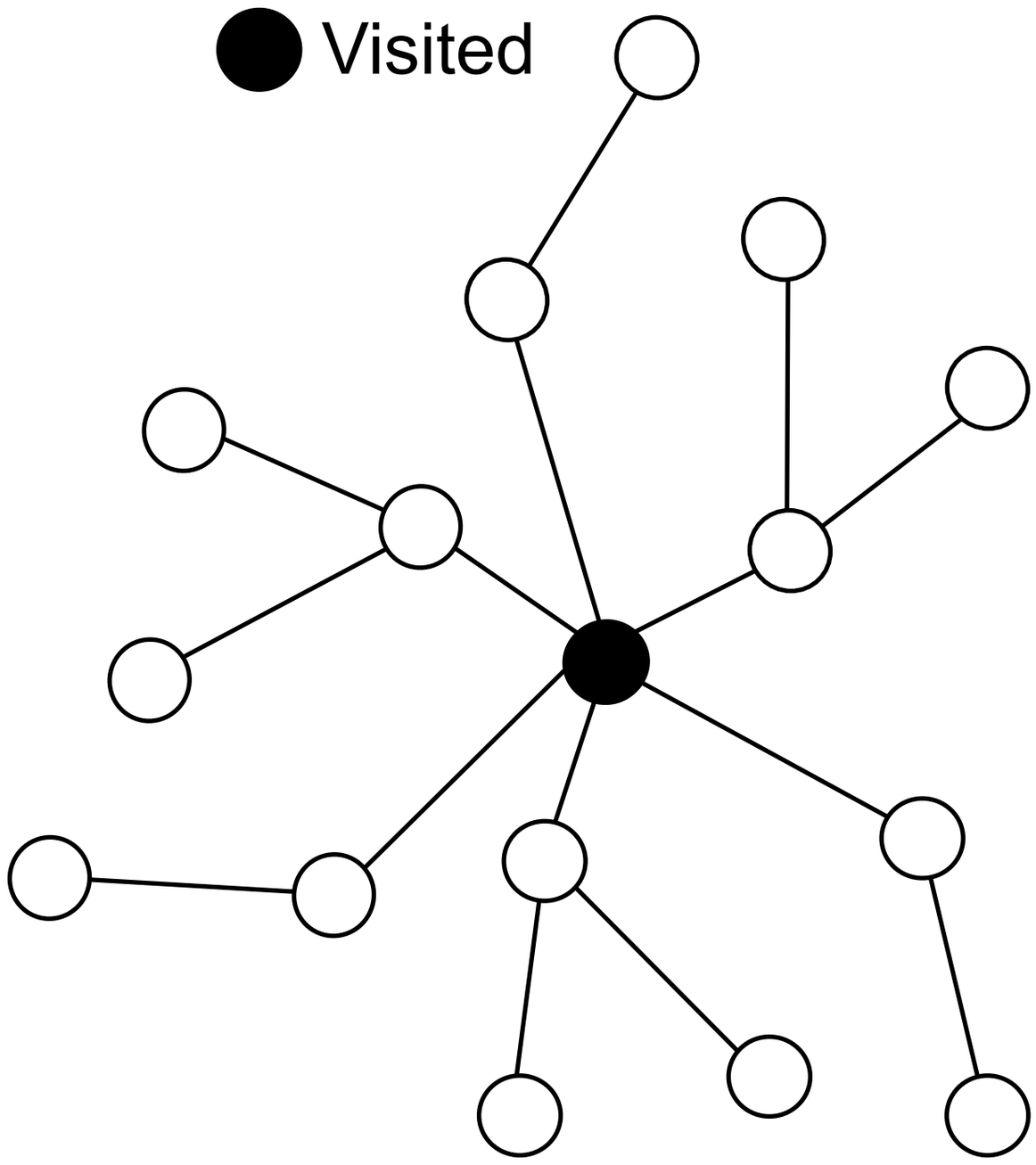

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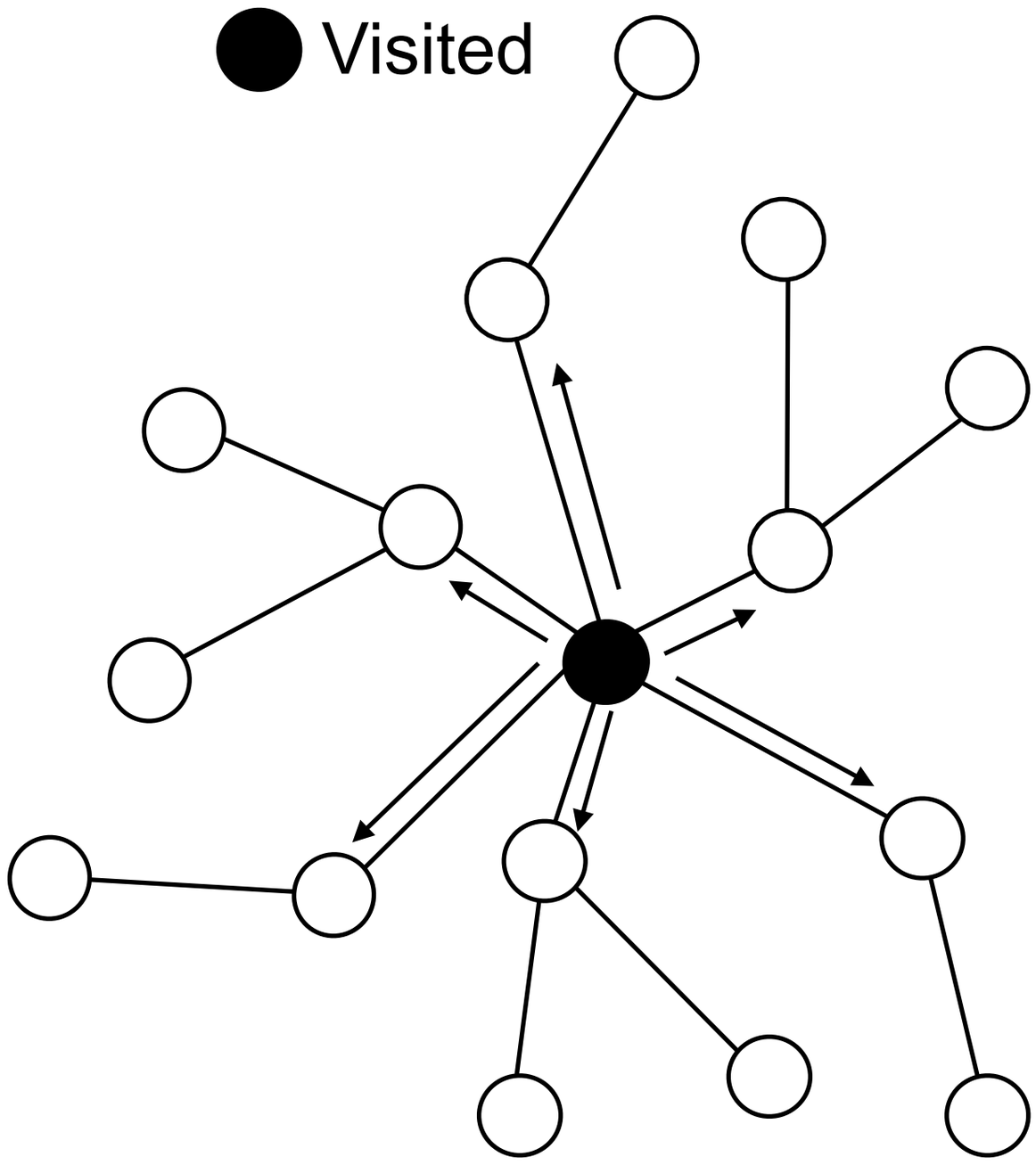

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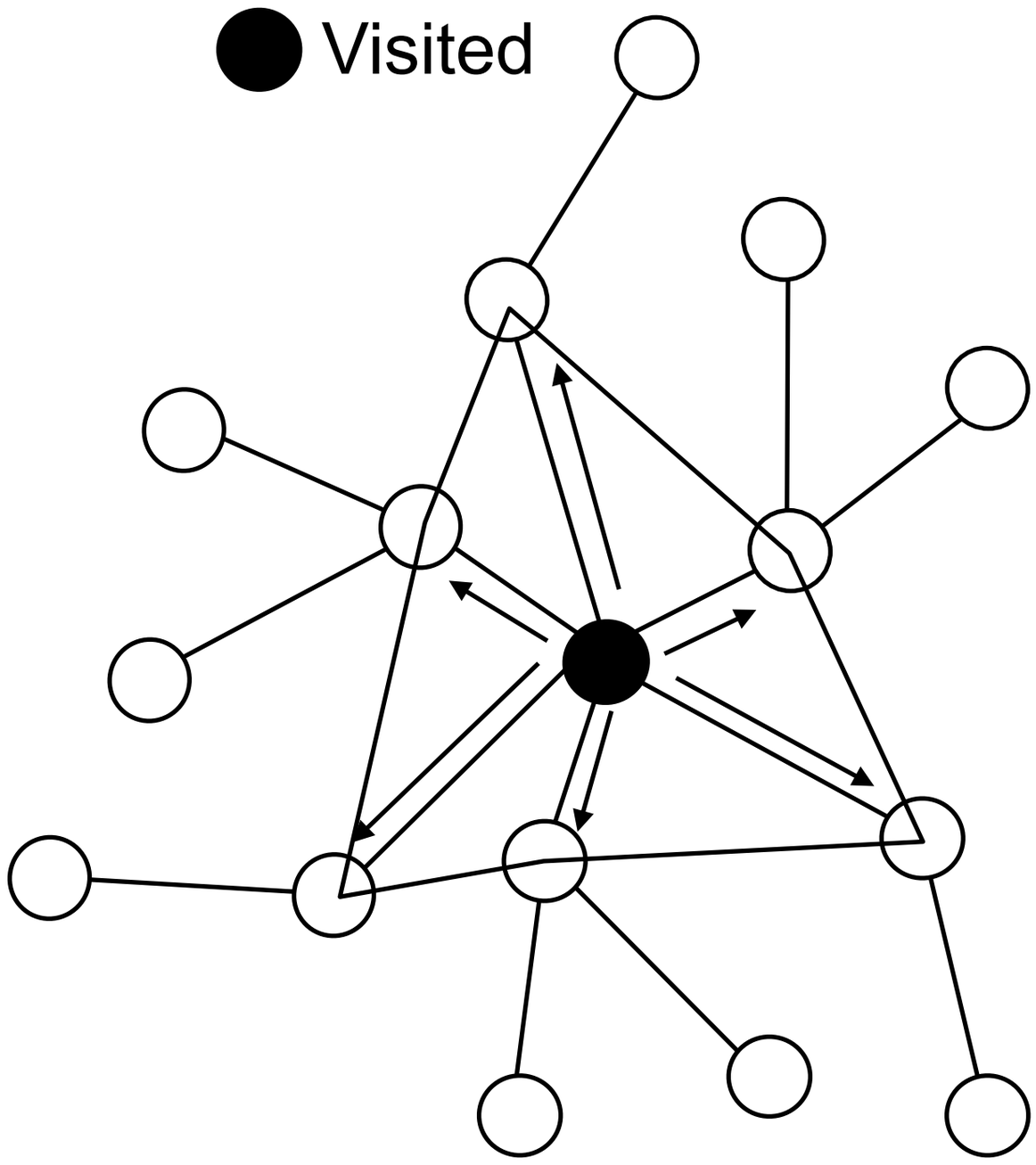

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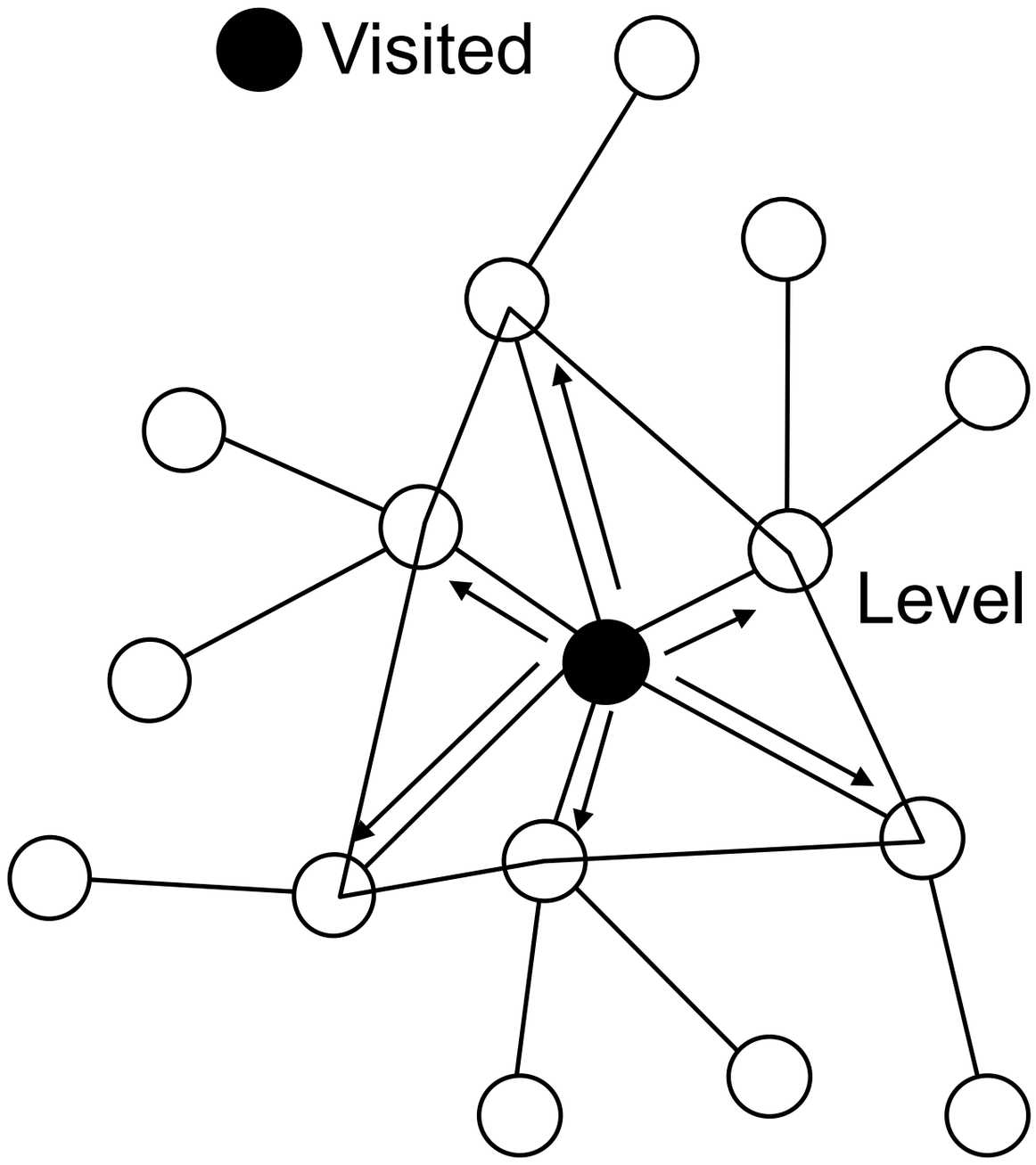

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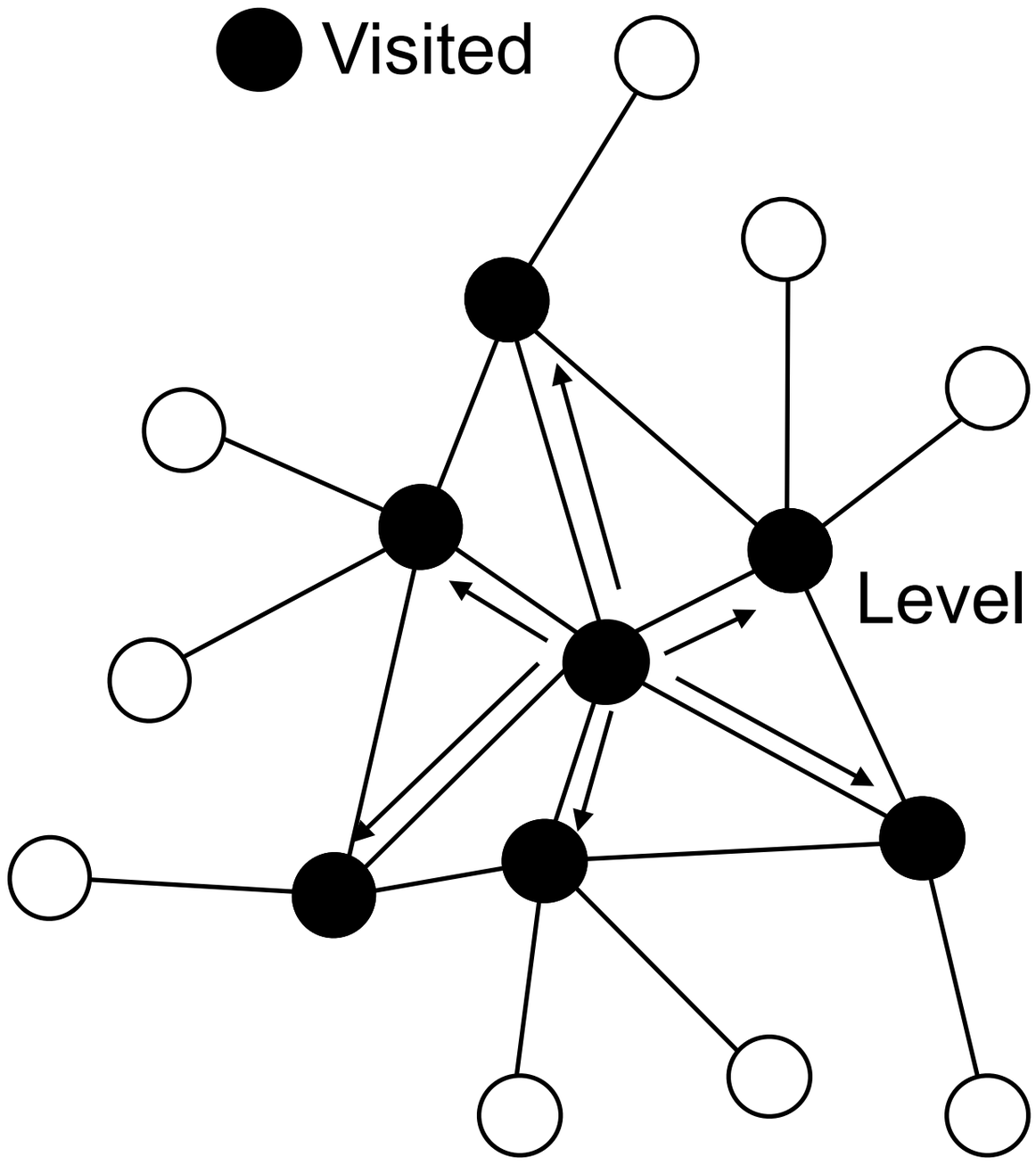

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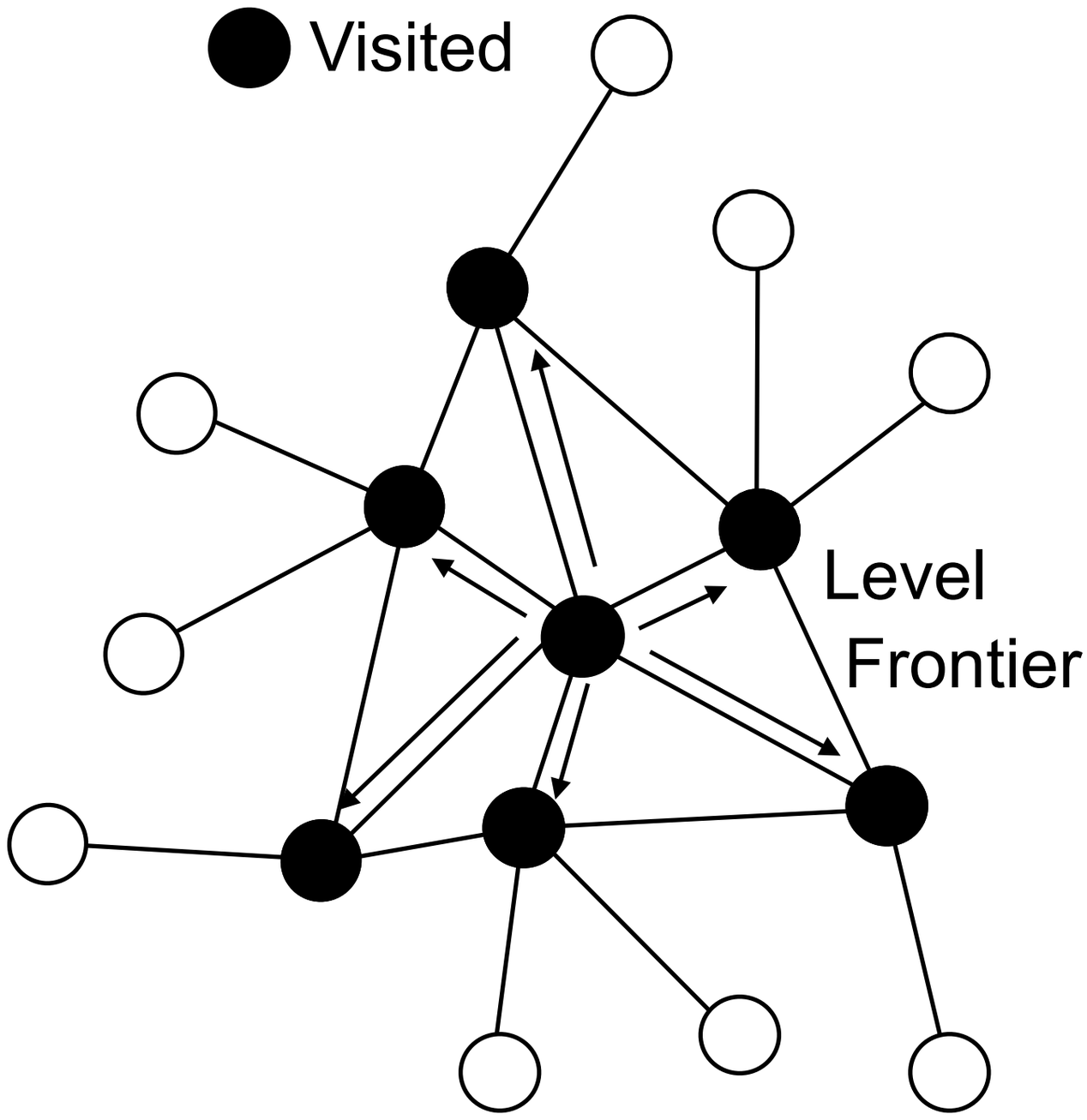

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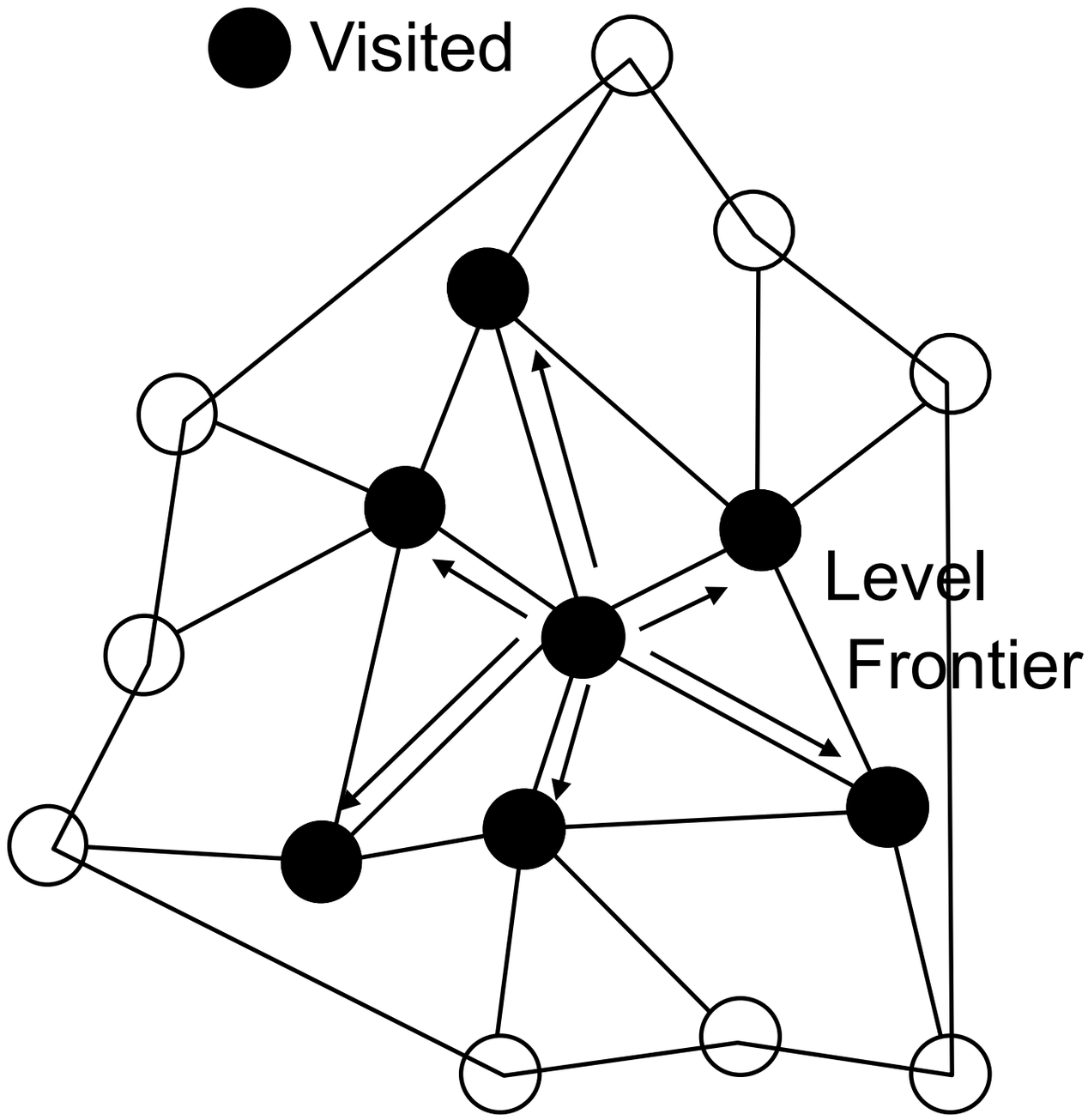

Power Problem on Servers

- Performance has been improved as the amount of hardware resources is increased
- Power consumption also continues to grow
  - Proportional to # of active transistors
- One of the most critical design constraints

Summary of This Work

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- Contributions:
  - Investigate the memory access pattern of its main algorithm using a simulator
  - Reveal that conventional address mapping schemes of memory controllers do NOT efficiently exploit DRAM
  - Propose a novel scheme and improve DRAM power efficiency by 30.3%

Agenda

- State-of-the-art BFS implementation
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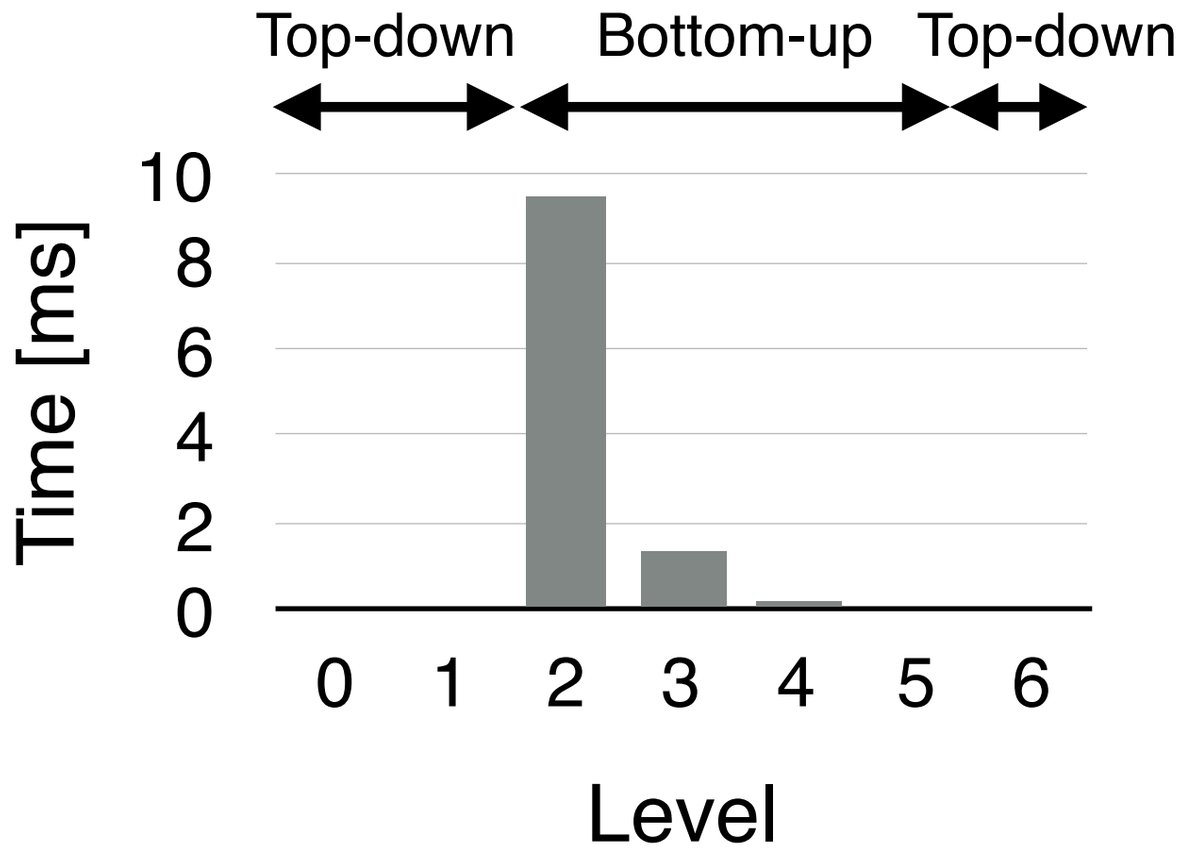
Yasui16 Implementation

[Yasui+, HPGP'16]

- Achieved the best performance for a single-node system in the June 2016 Graph500 list

- Applies several tuning techniques
  - NUMA-aware data layout [Yasui+, BigData'13]
  - Adjacency list and vertex sorting [Yasui+, HPCS'15]
  - Direction optimizing [Beamer+, SC'12]
    - ✓ Significantly reduces # of edge traversals by switching two algorithms at each level: ***top-down*** or ***bottom-up***

Time Breakdown of BFS



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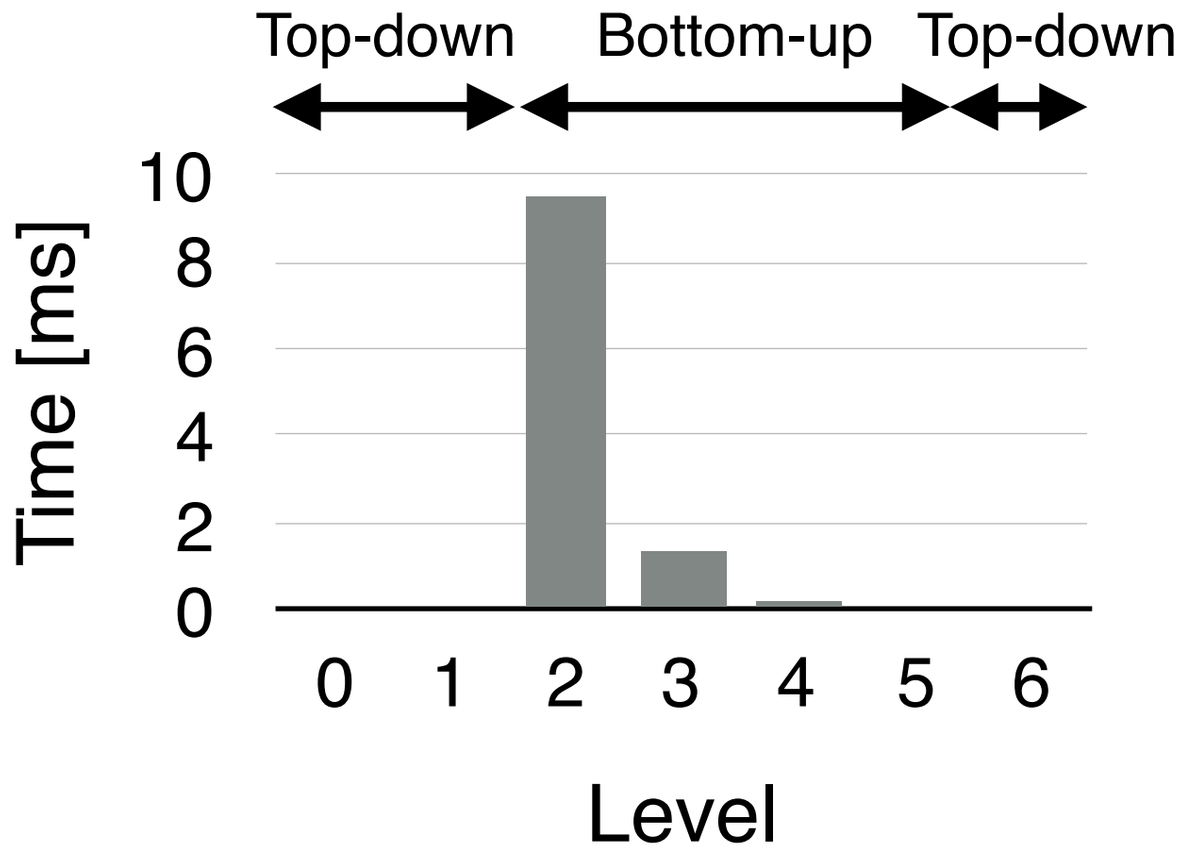

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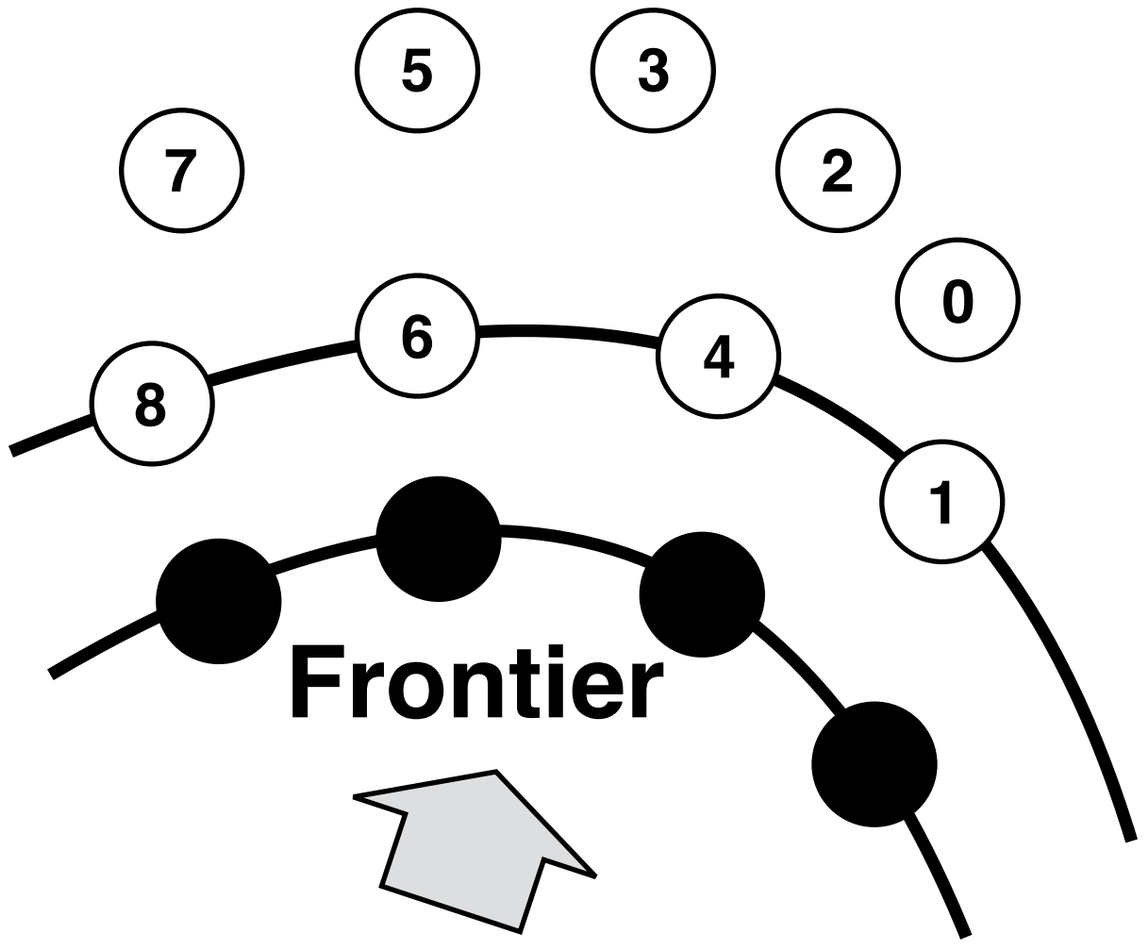
- Over 99% of exe. time is spent by bottom-up algorithm
- We aim to improve the power efficiency of bottom-up

Bottom-up Algorithm



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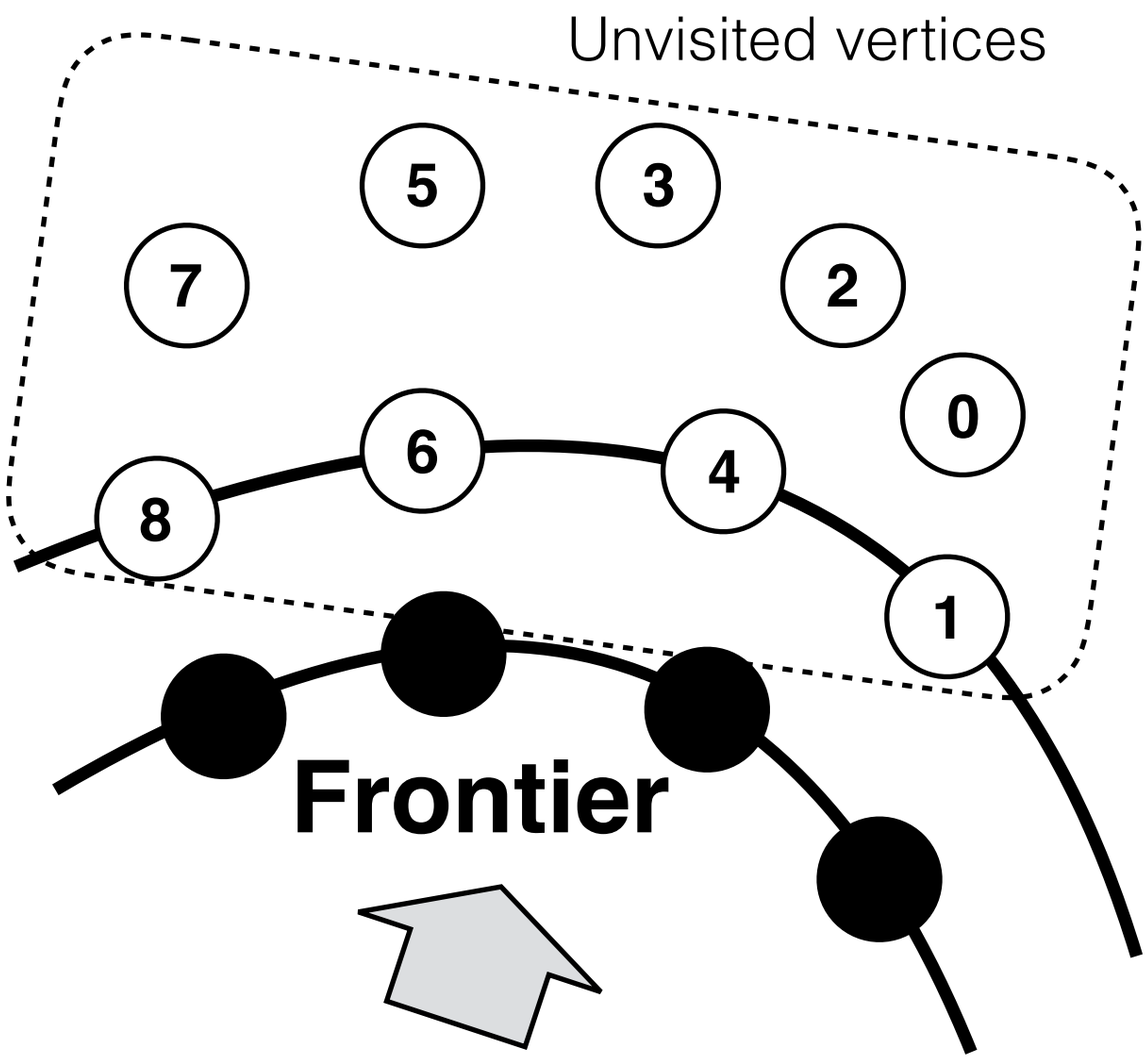

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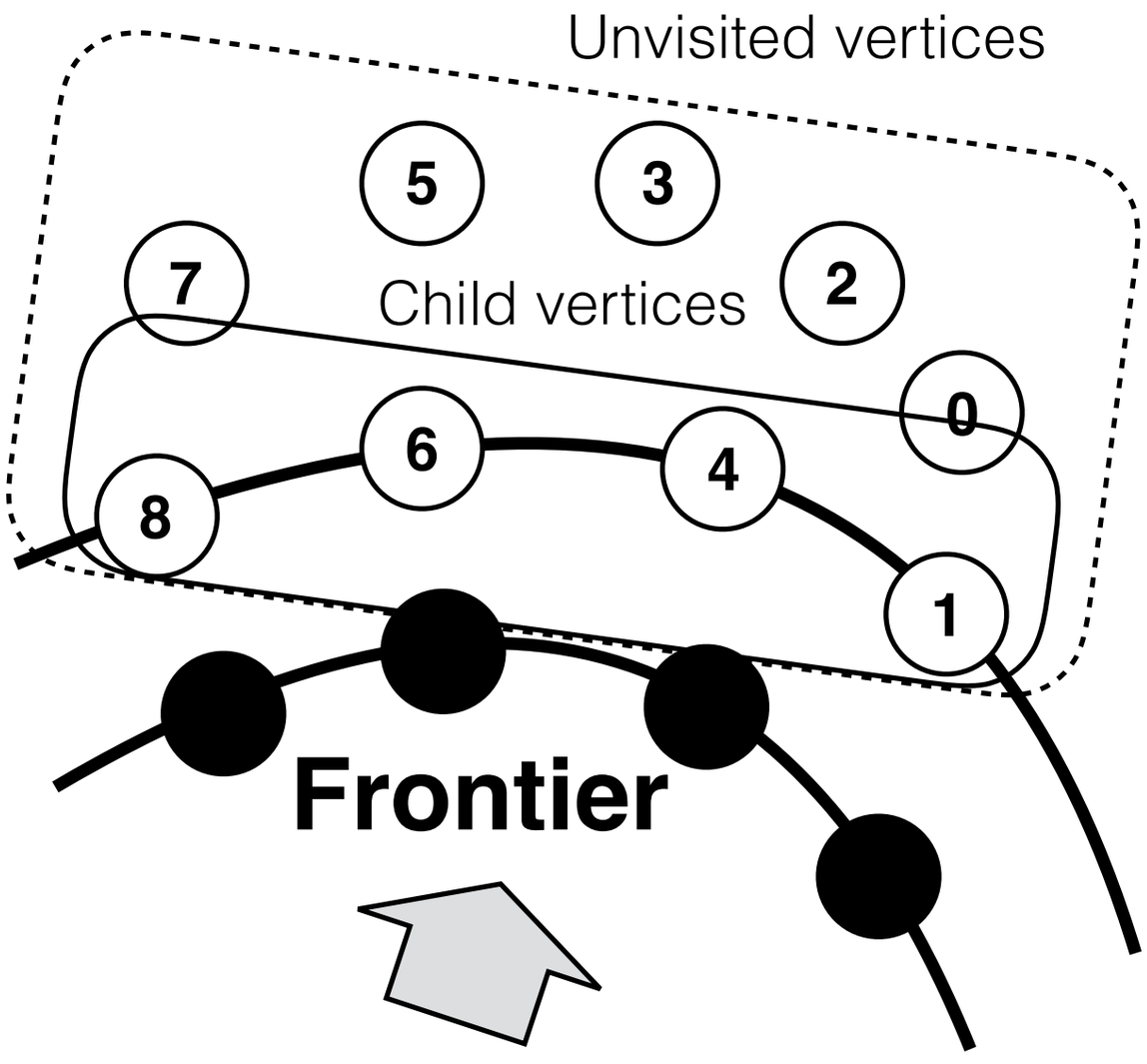

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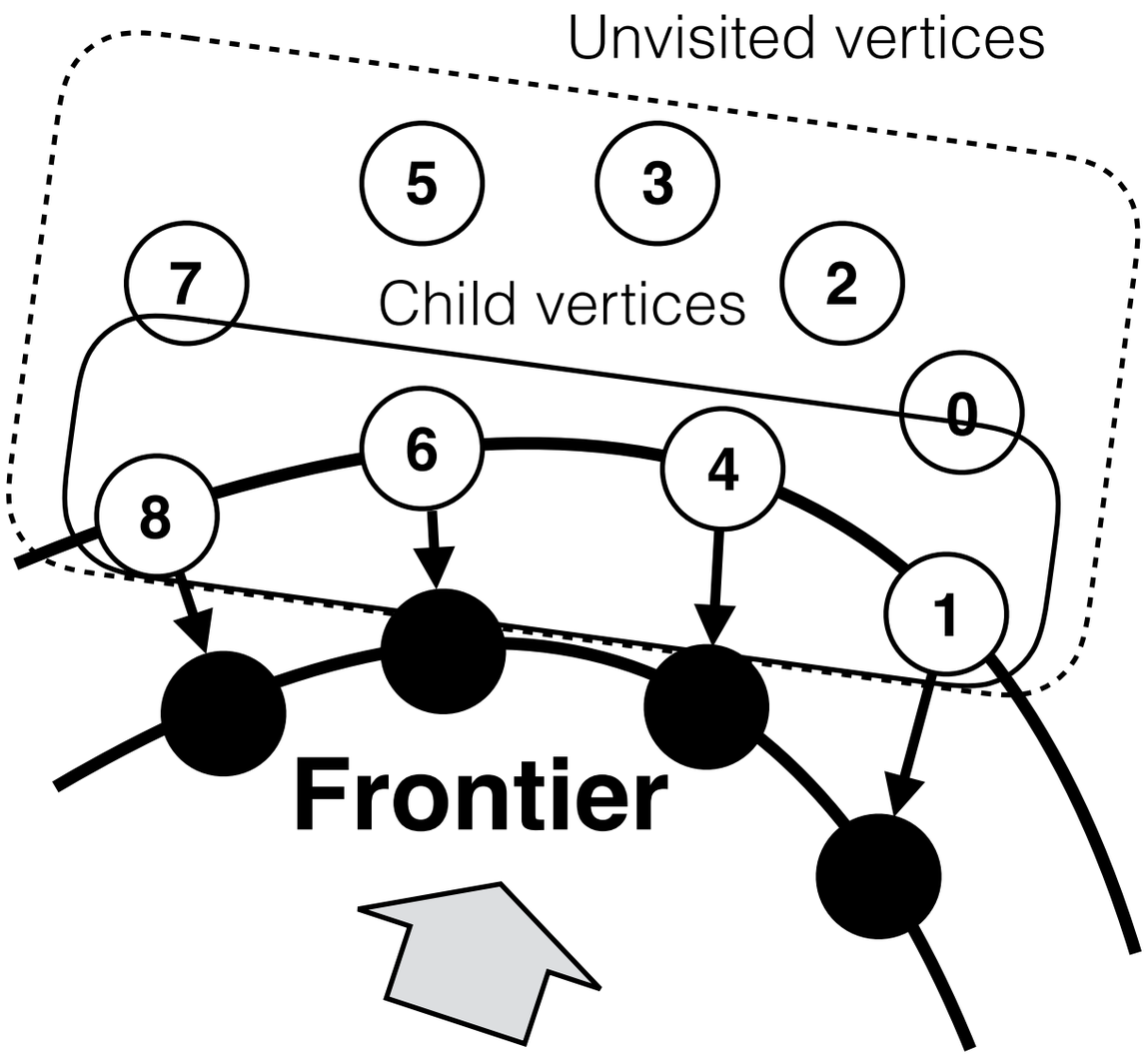

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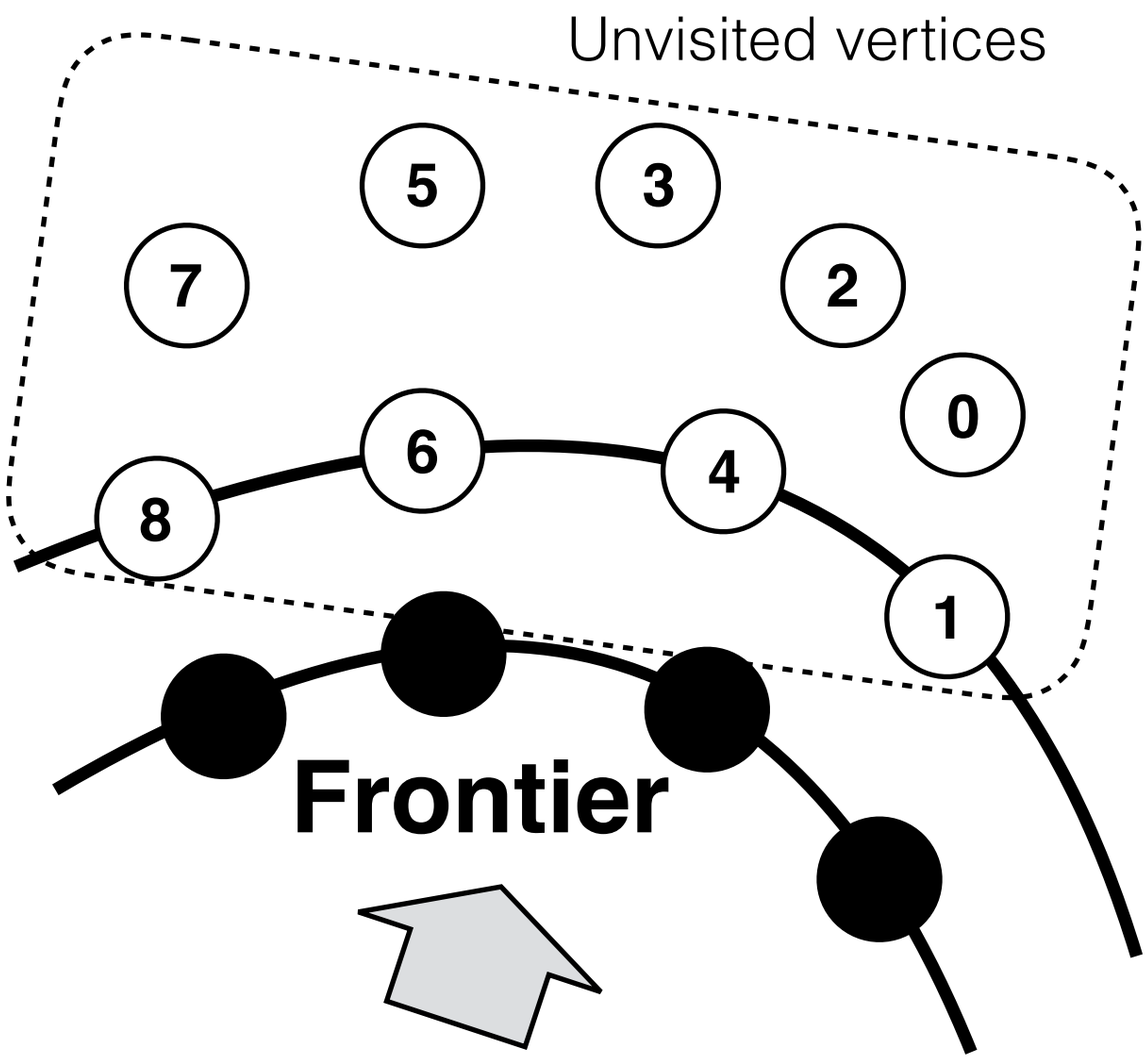

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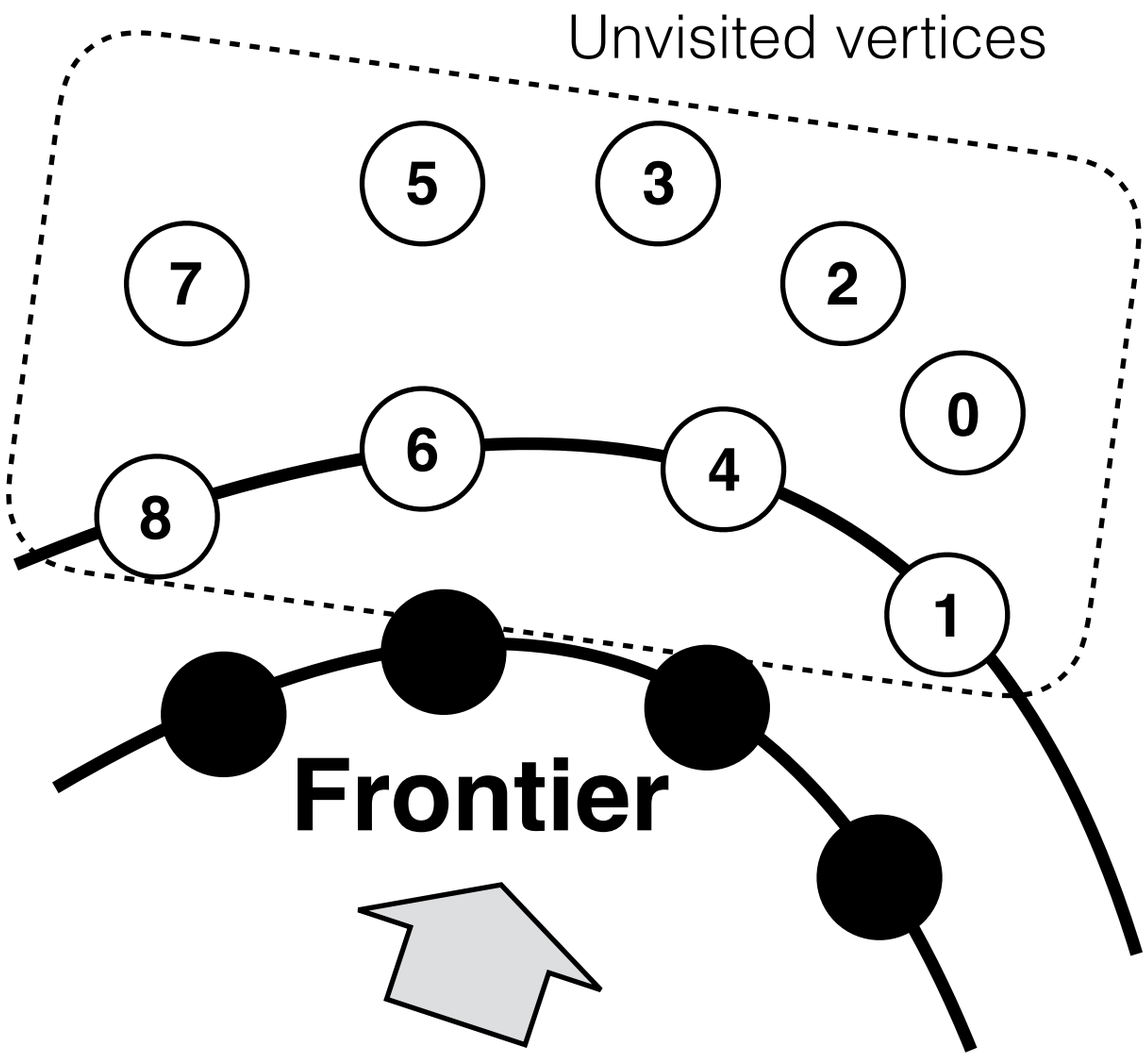

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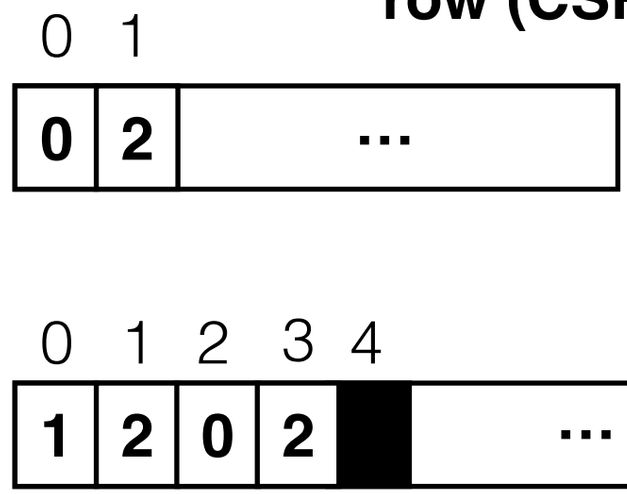

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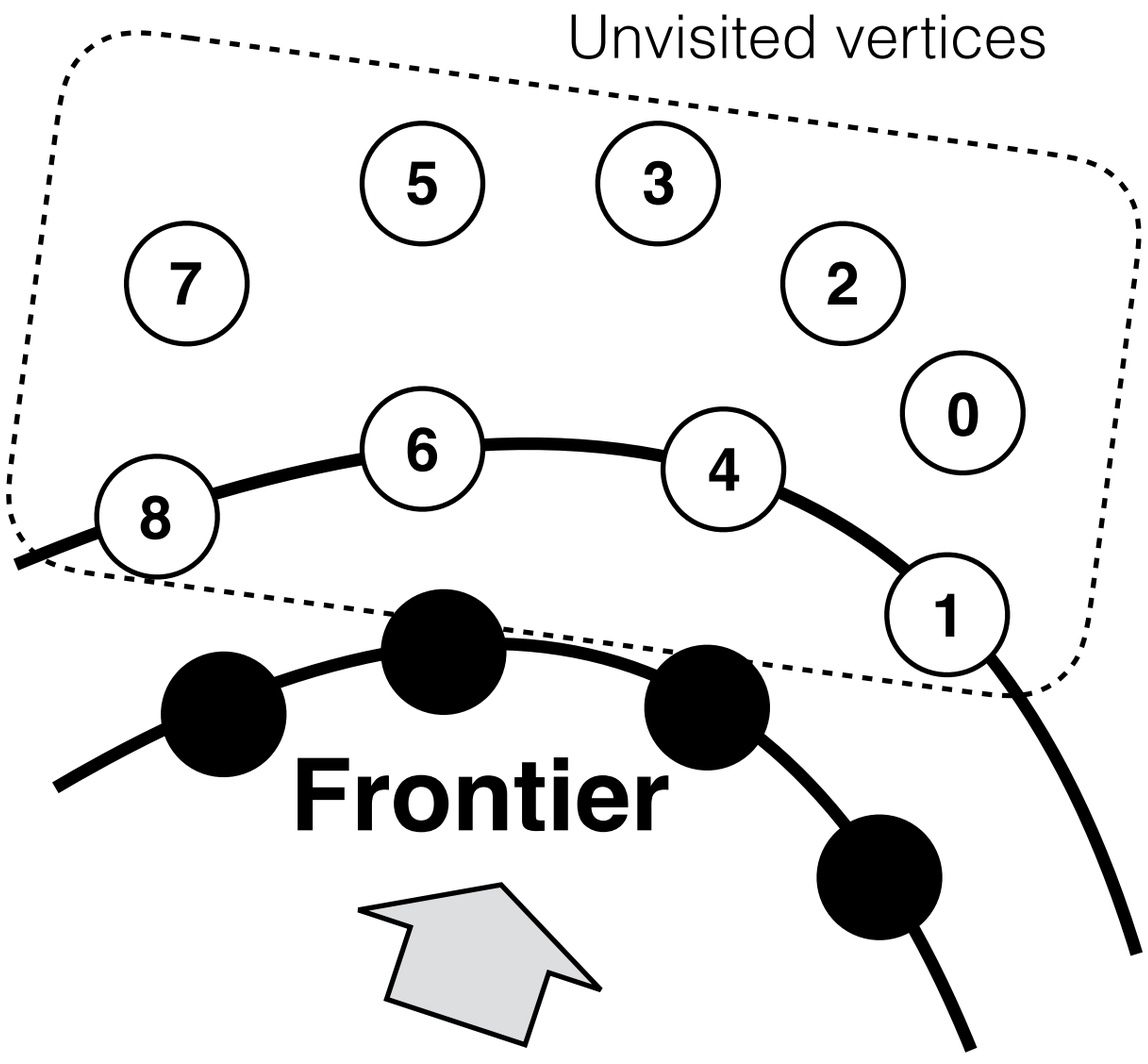

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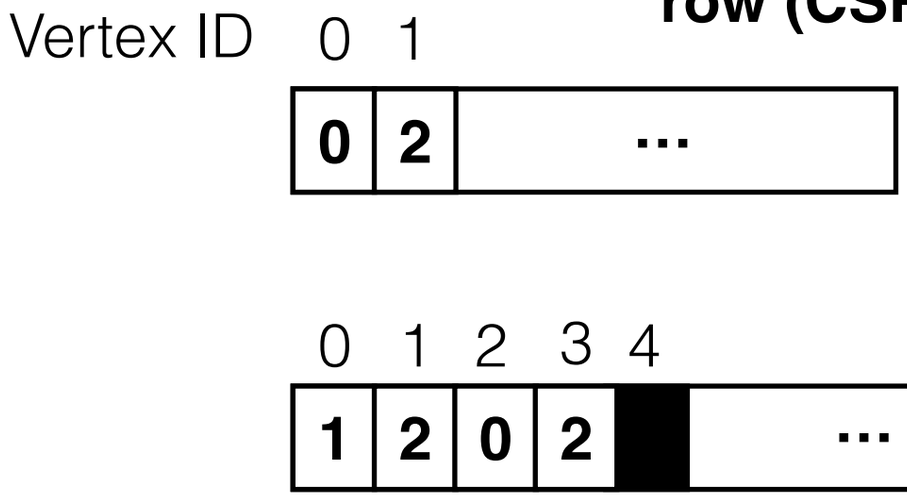

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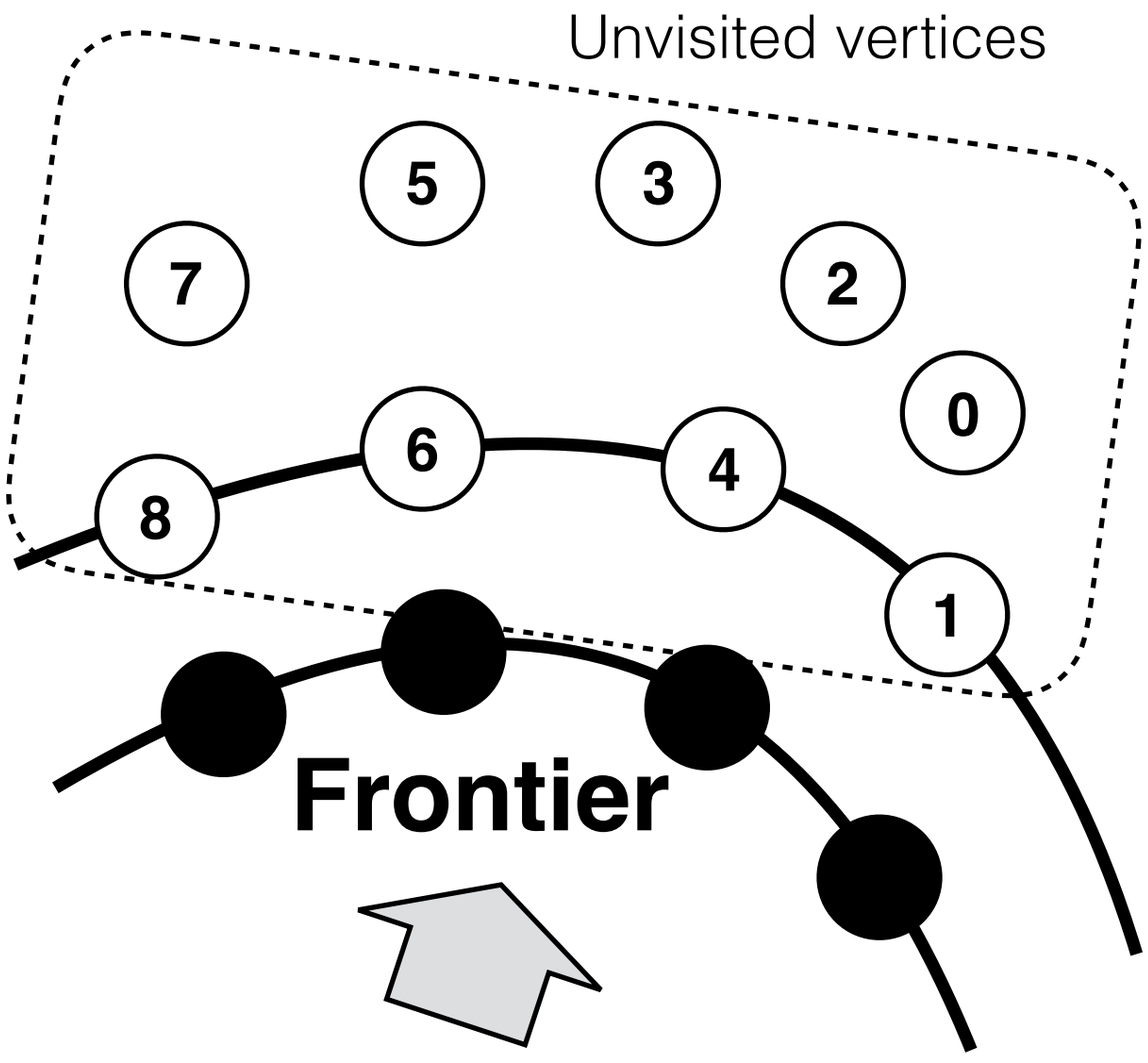

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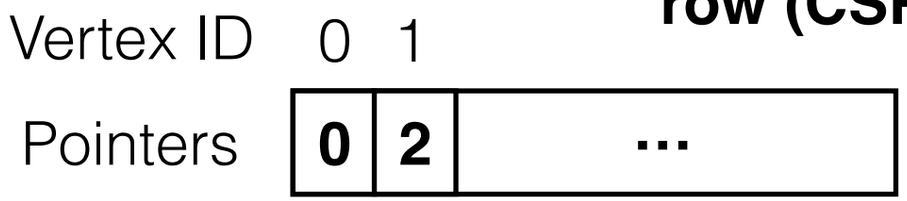

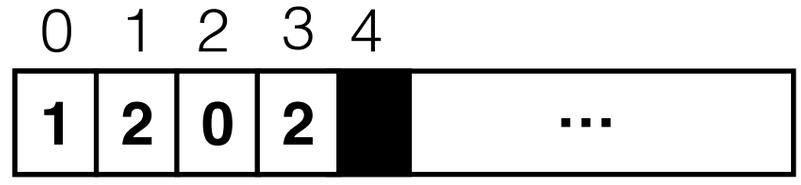

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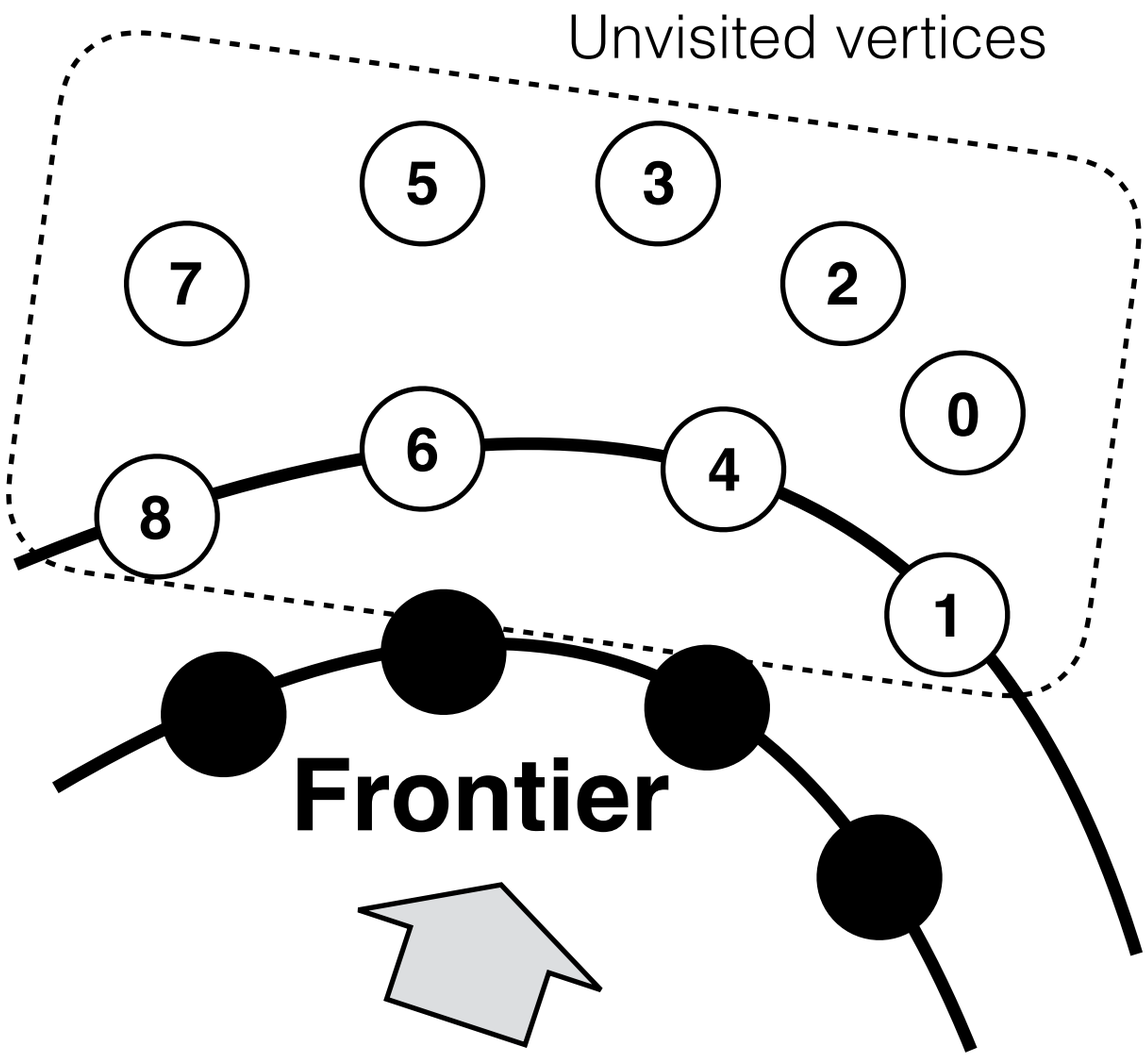

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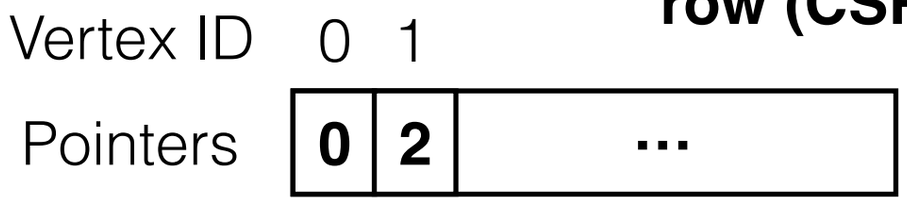

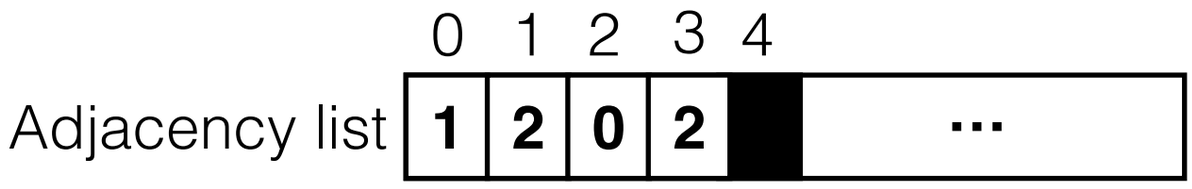

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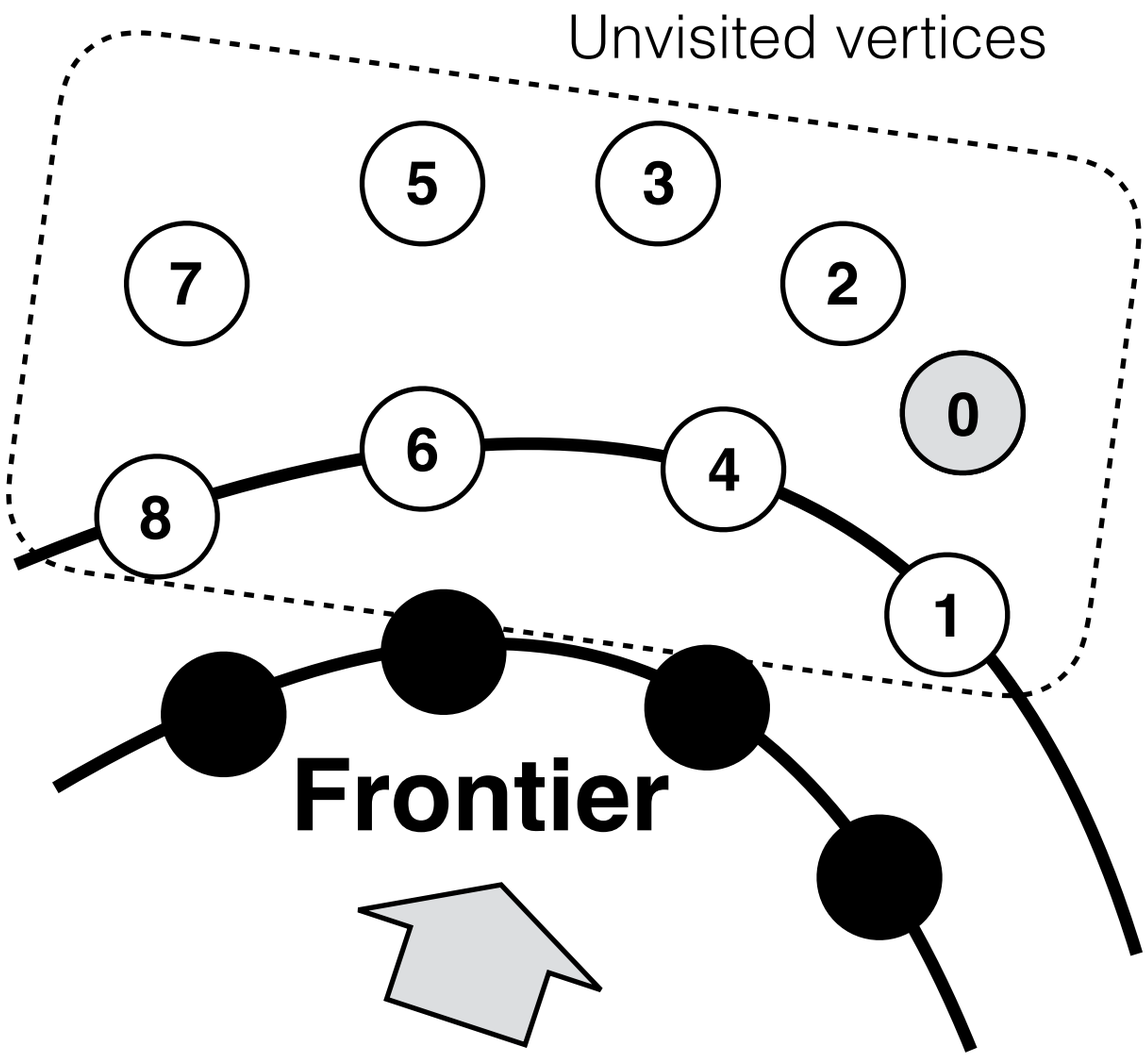

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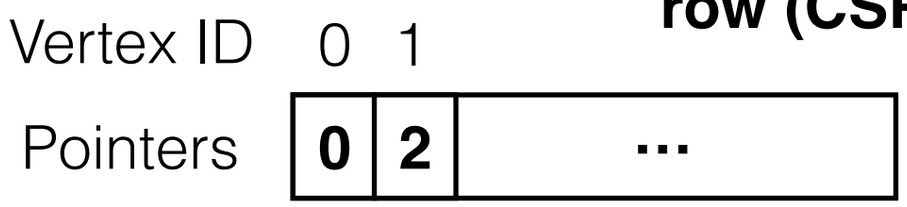

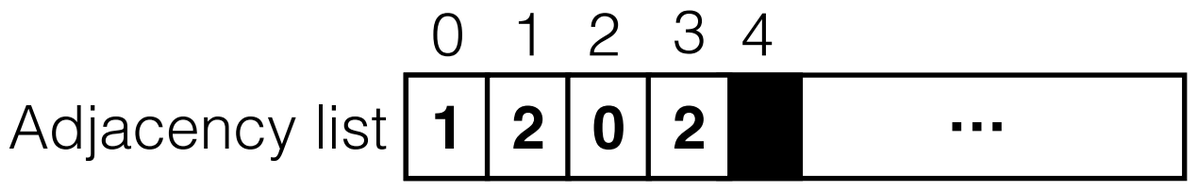

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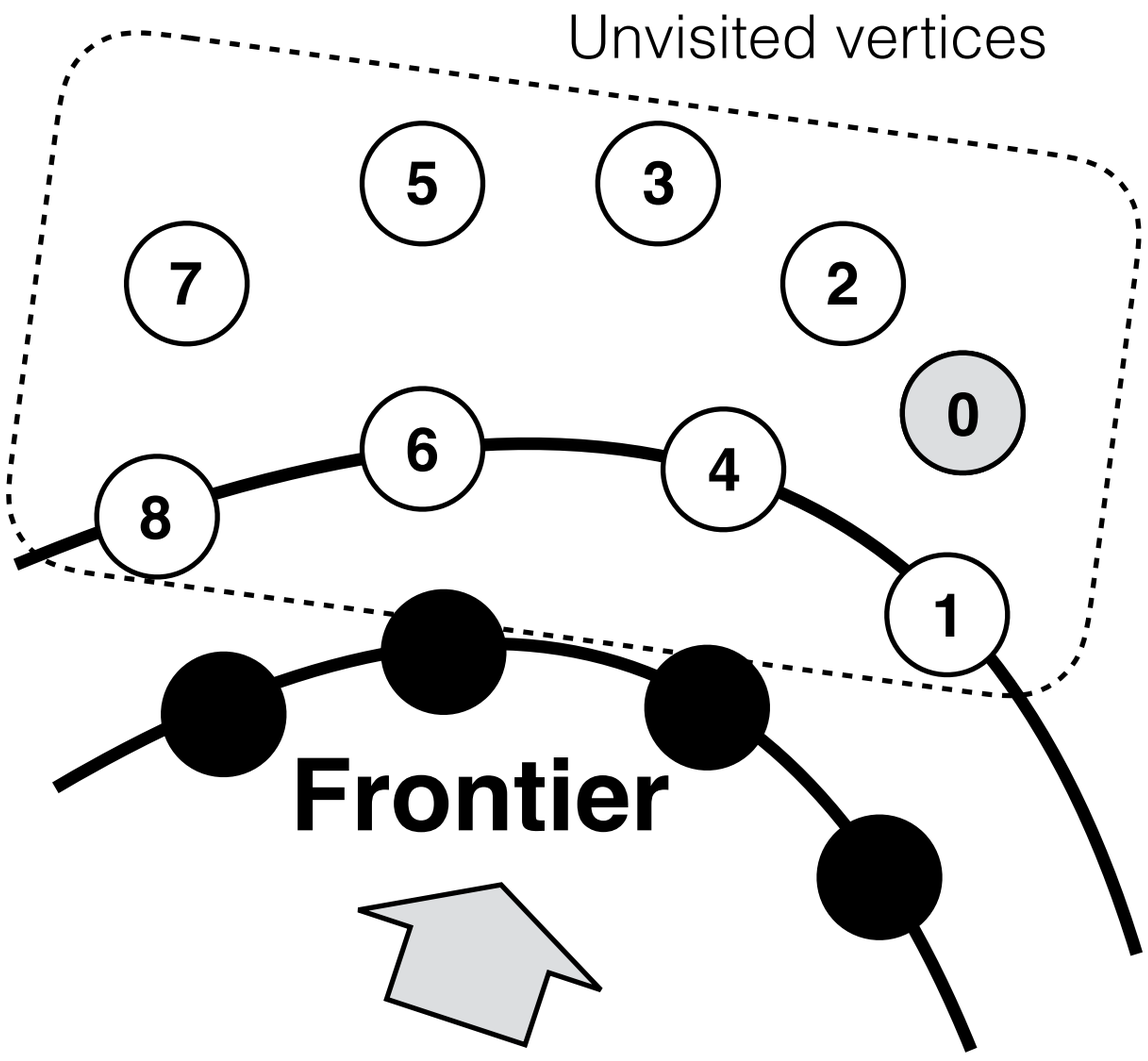

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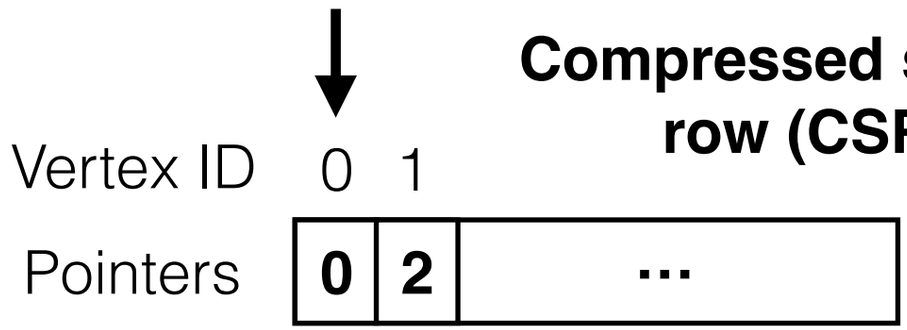

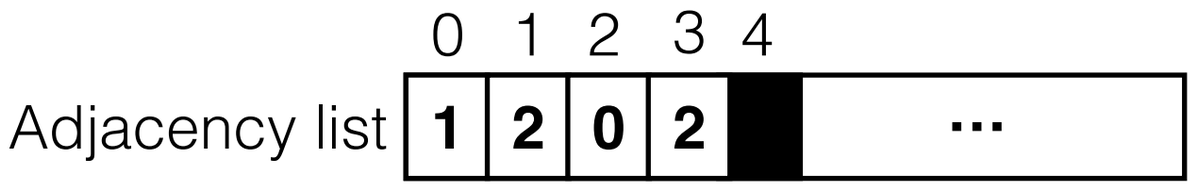

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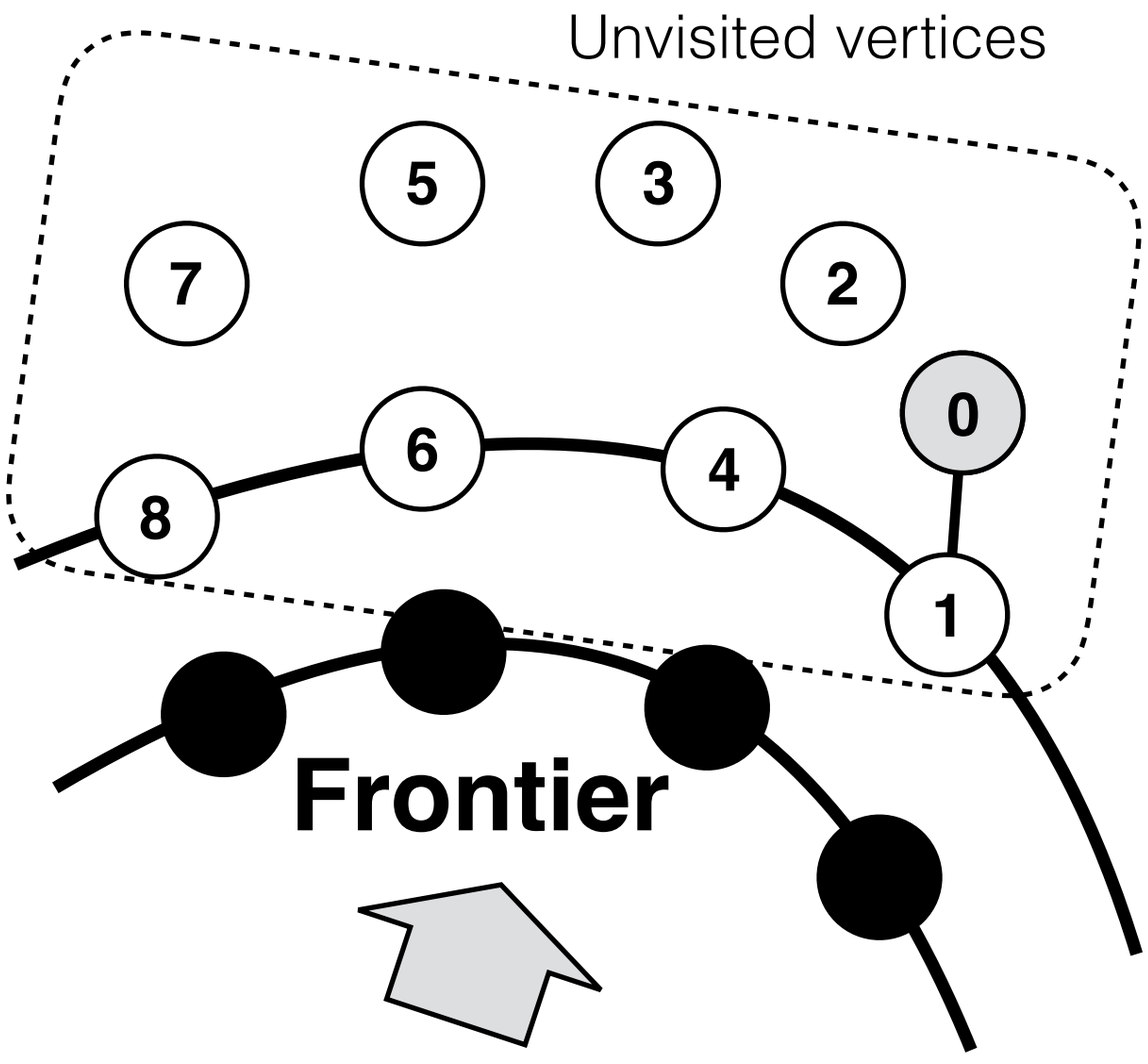

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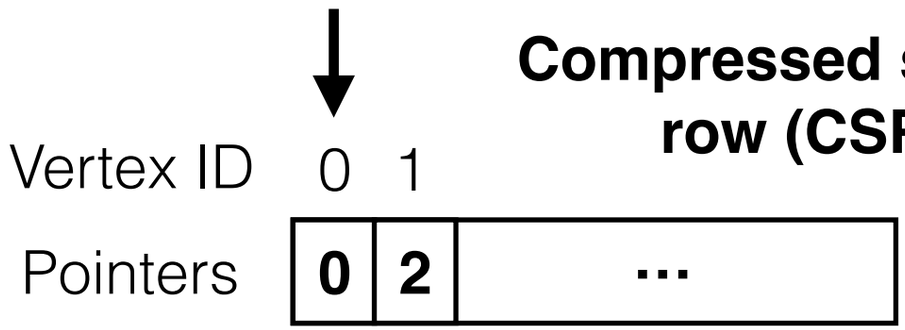

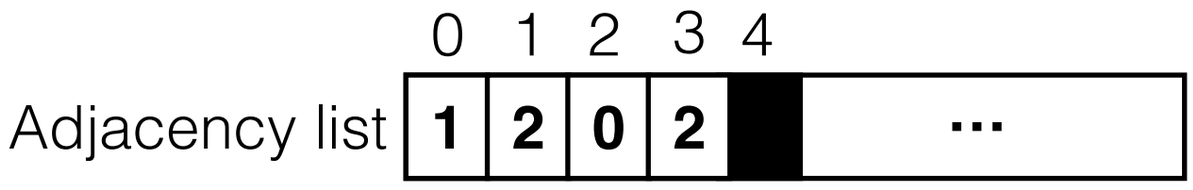

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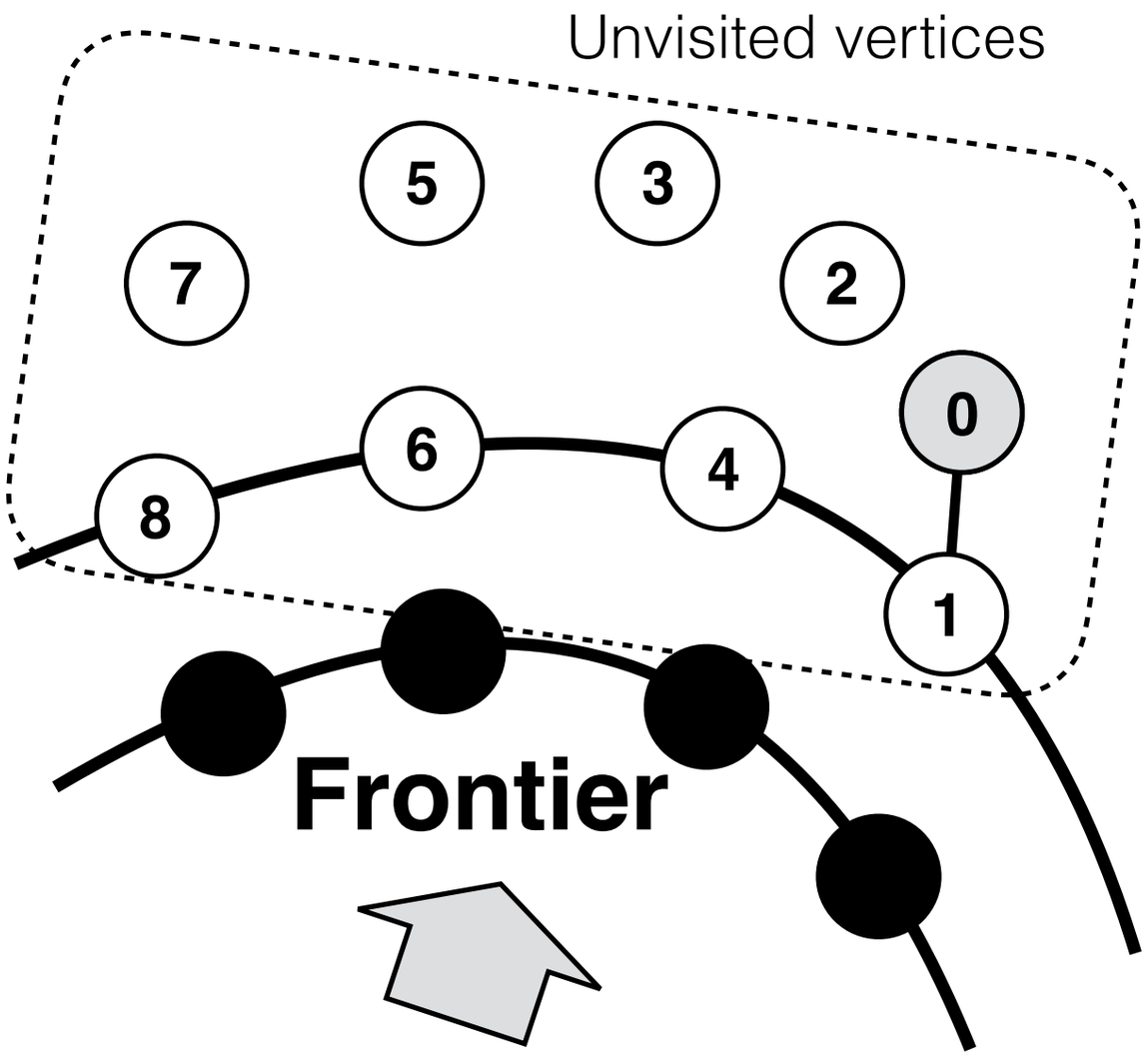

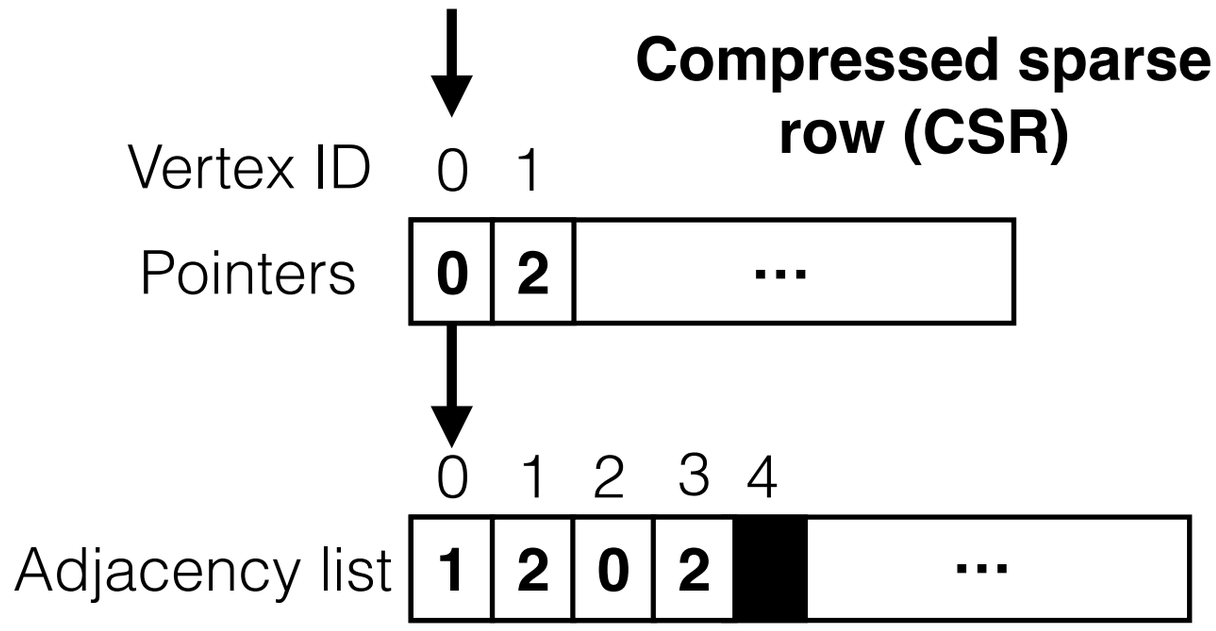

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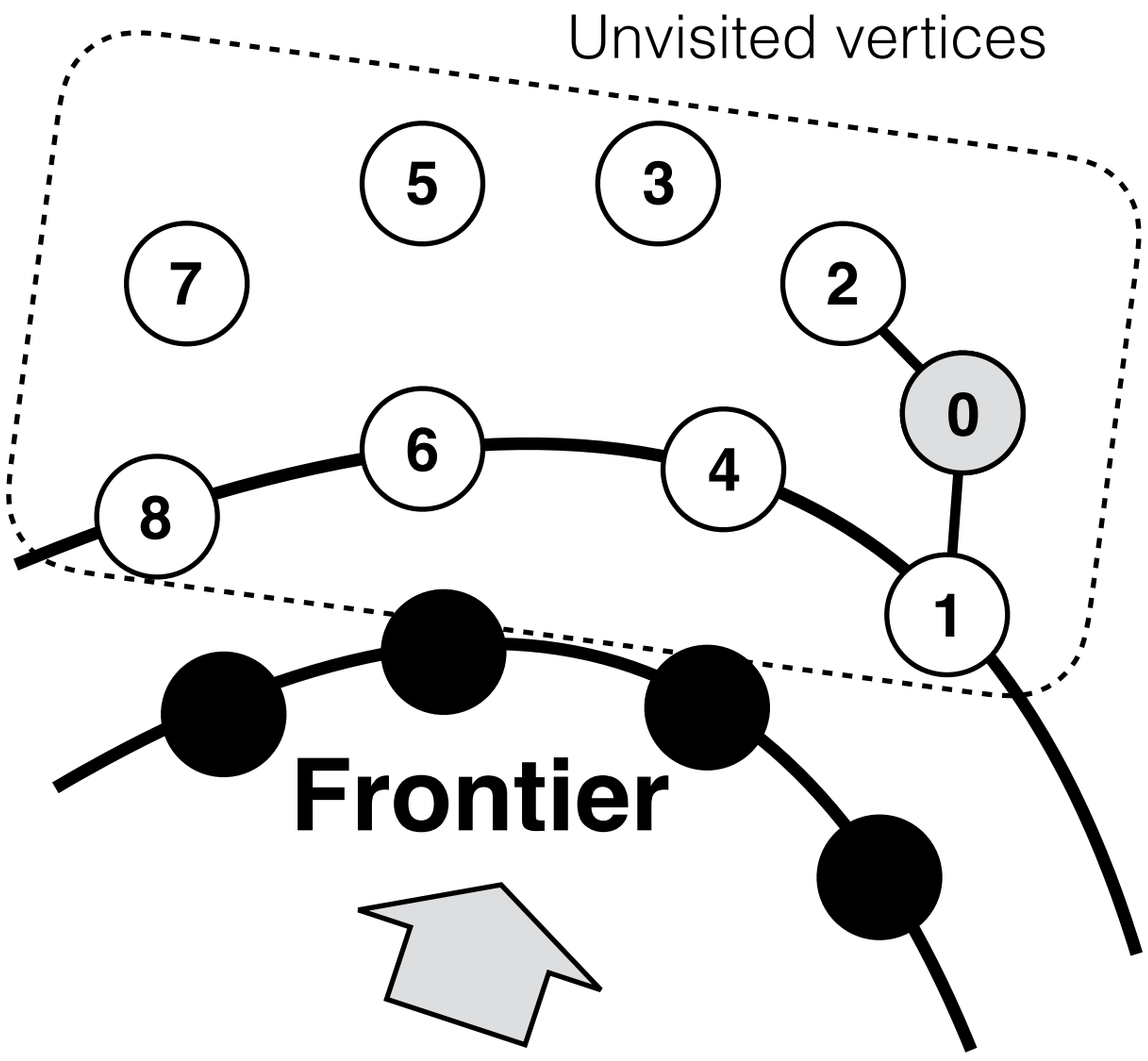

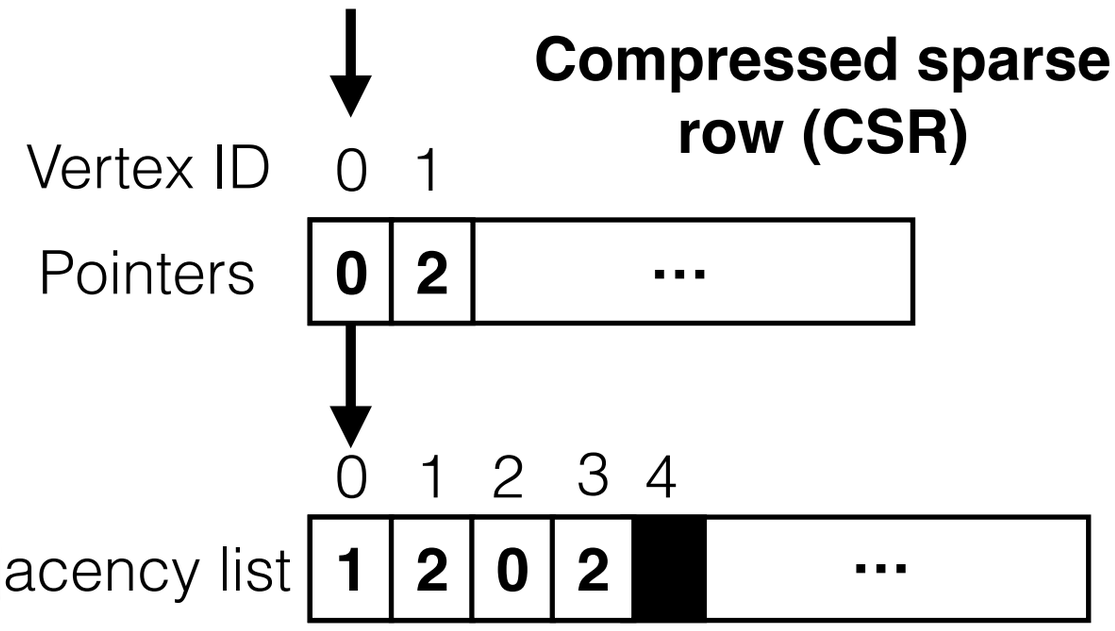

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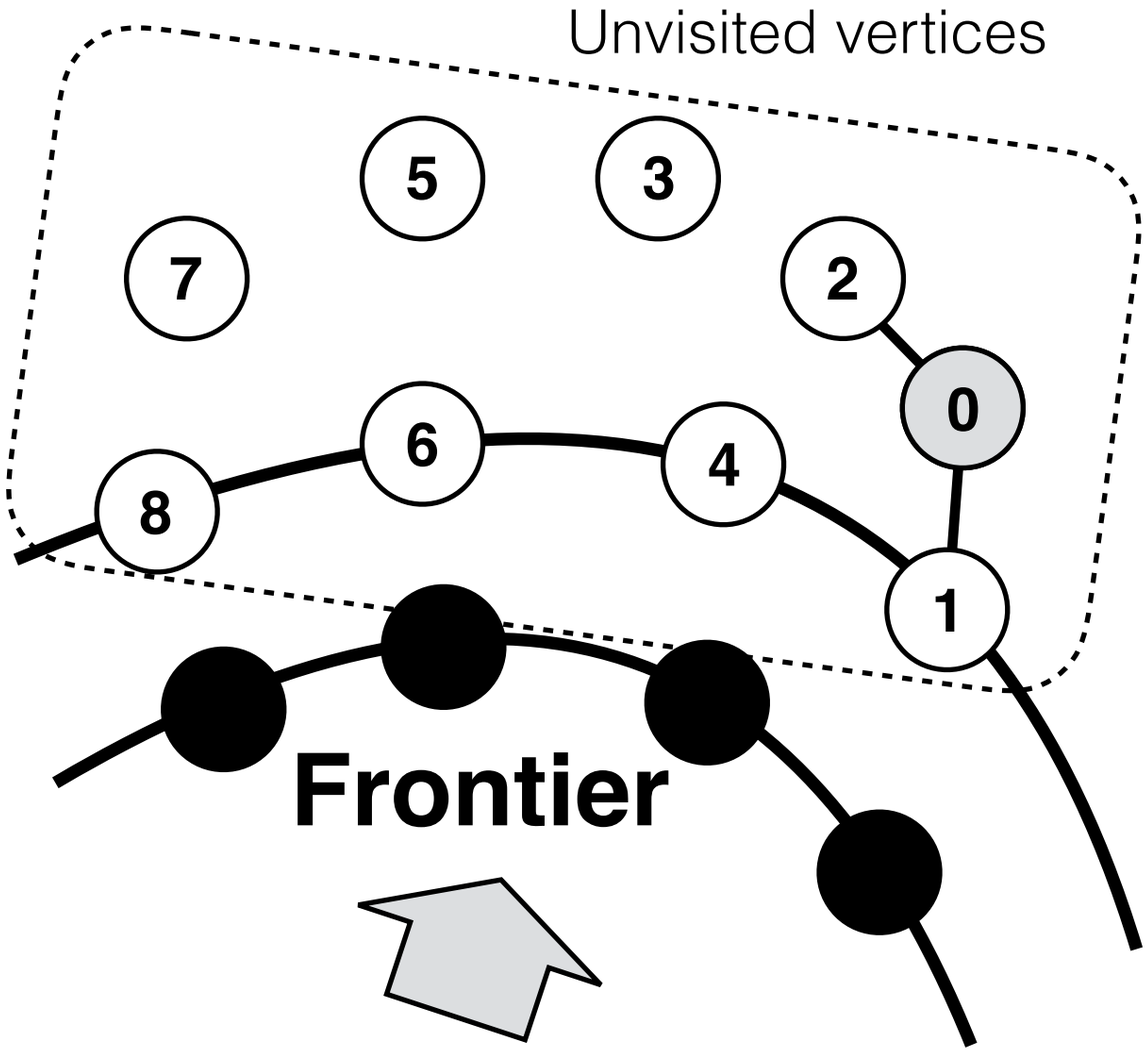

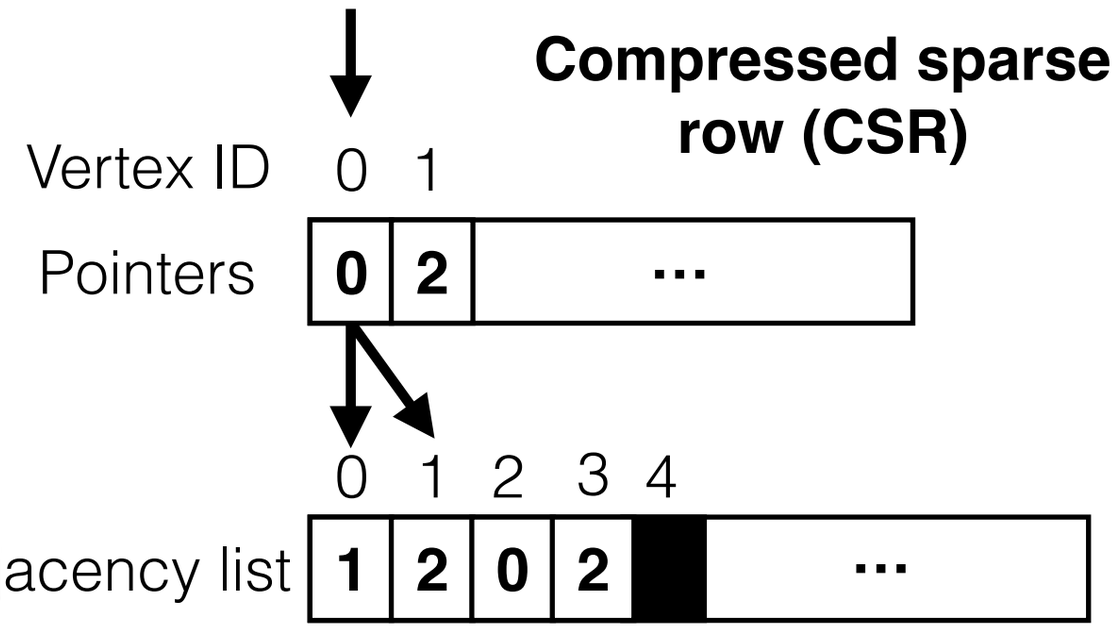

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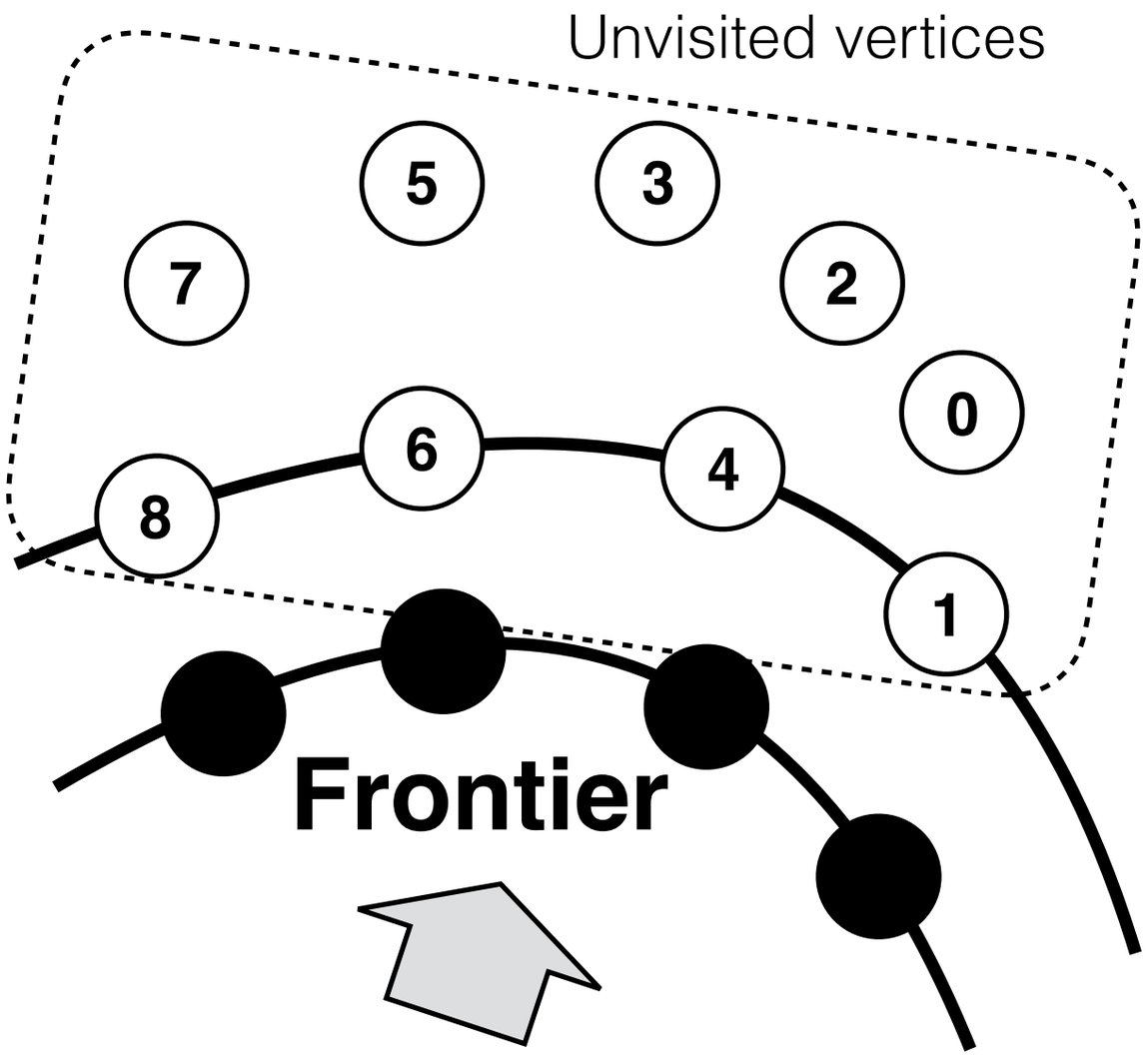

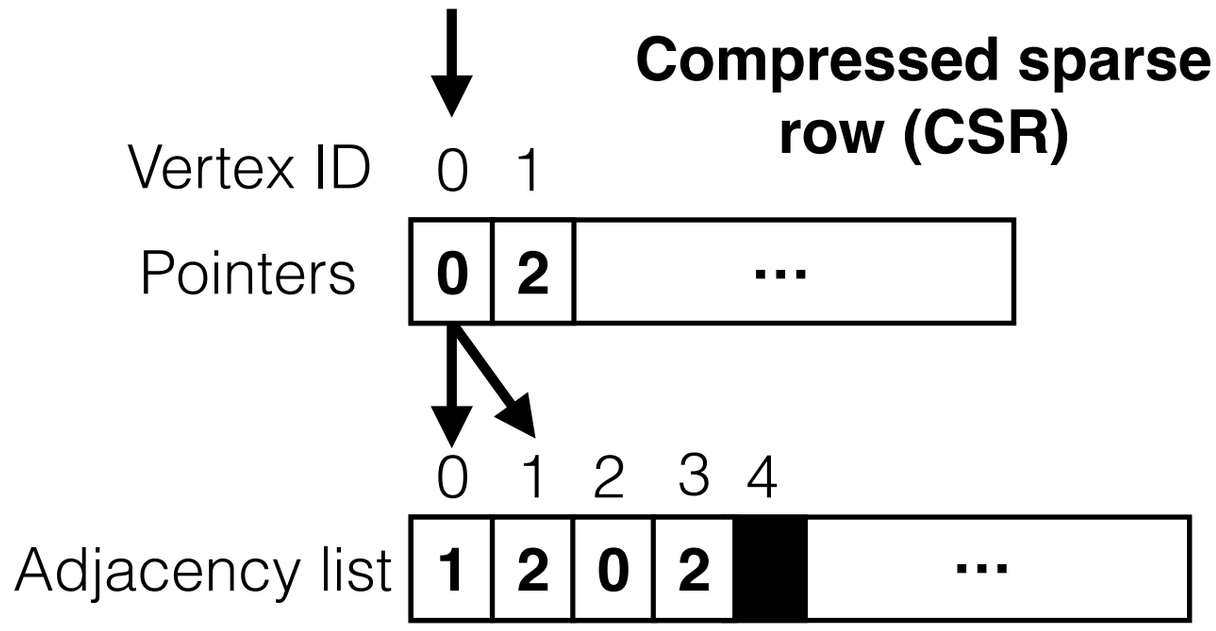

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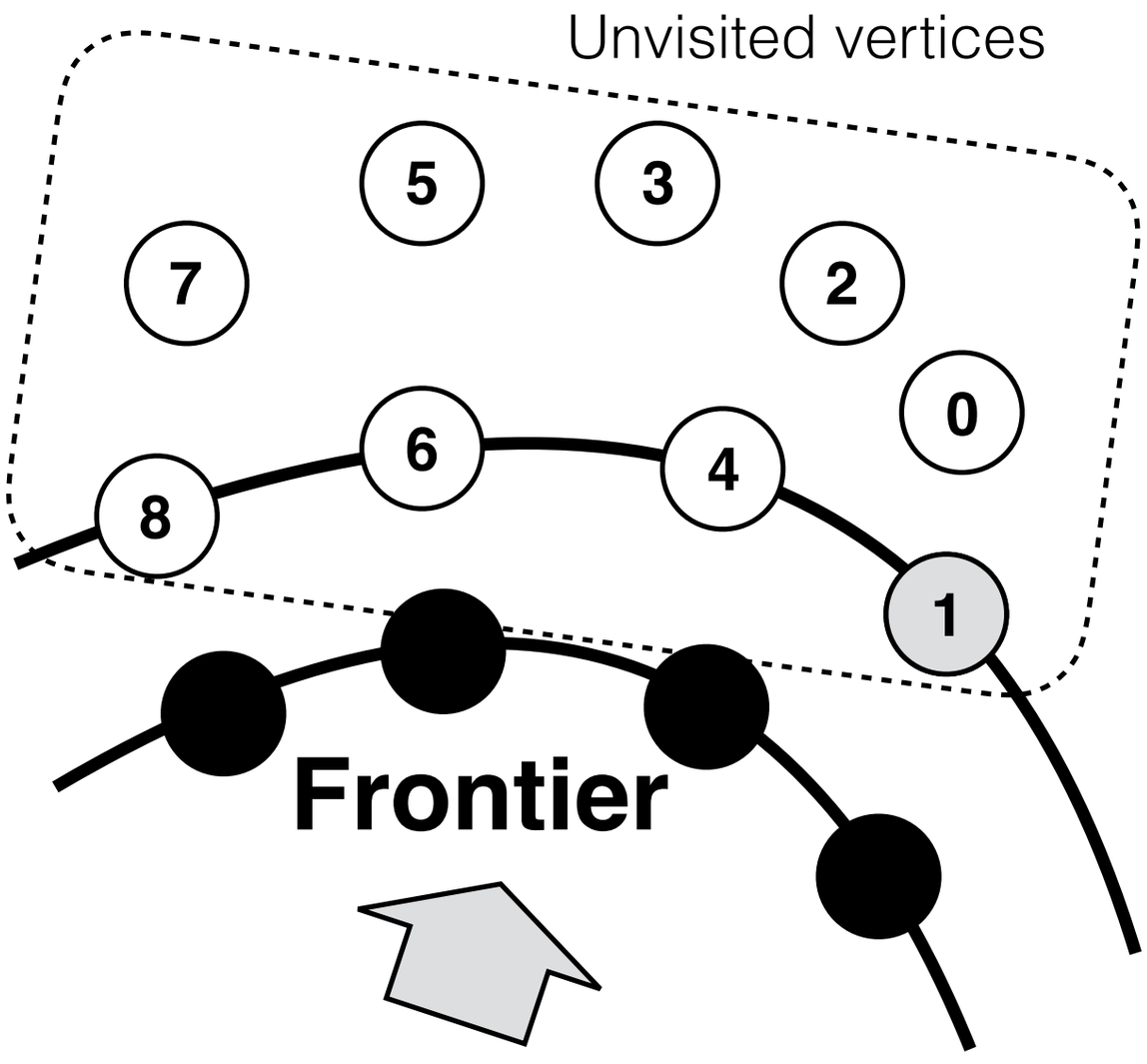

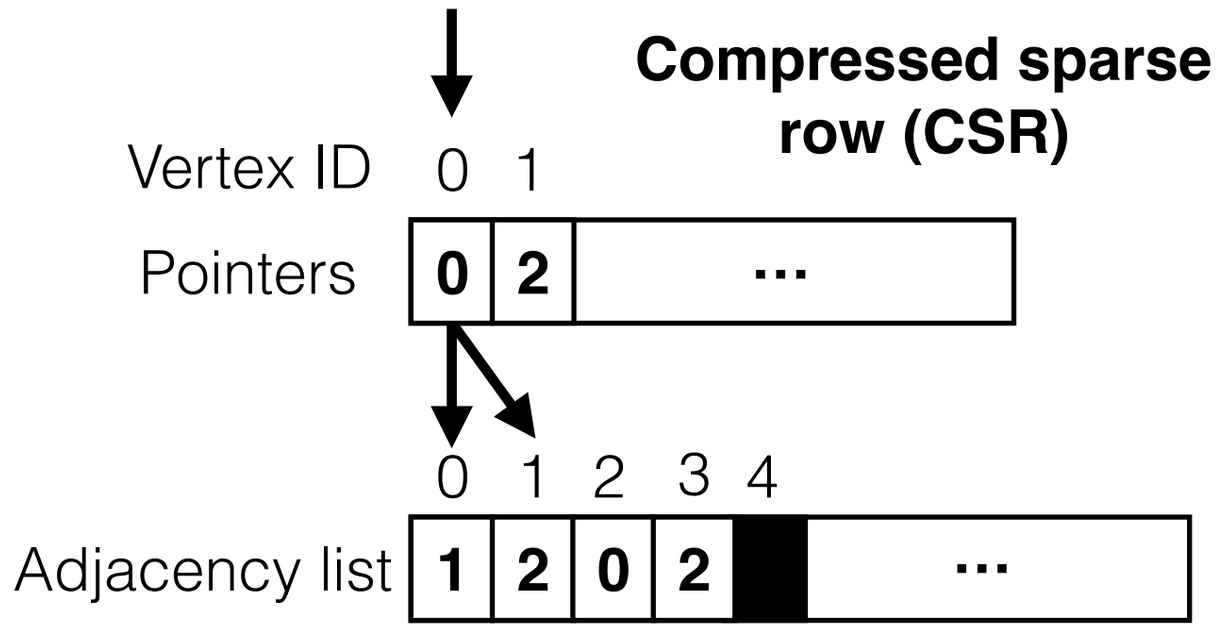

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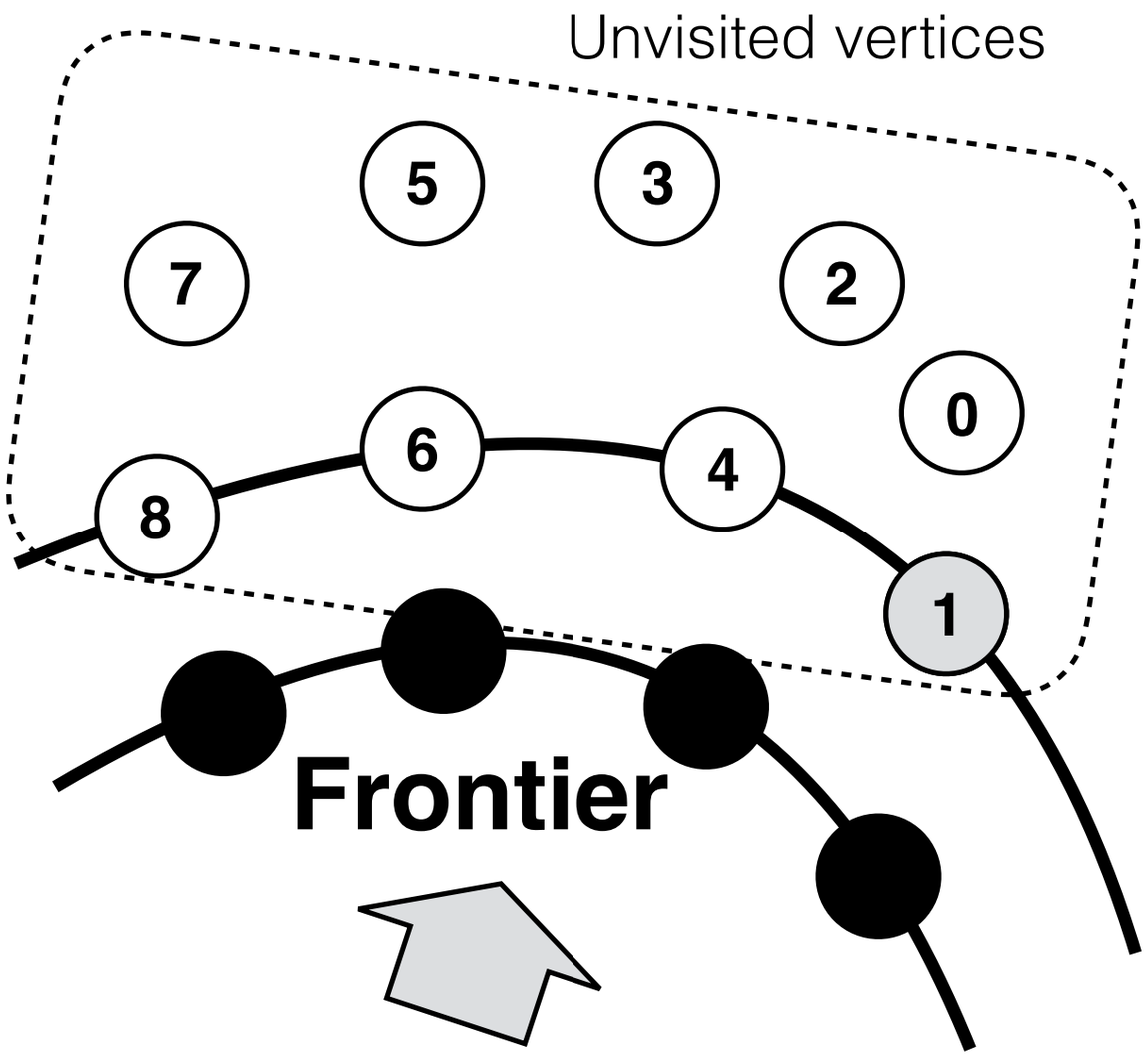

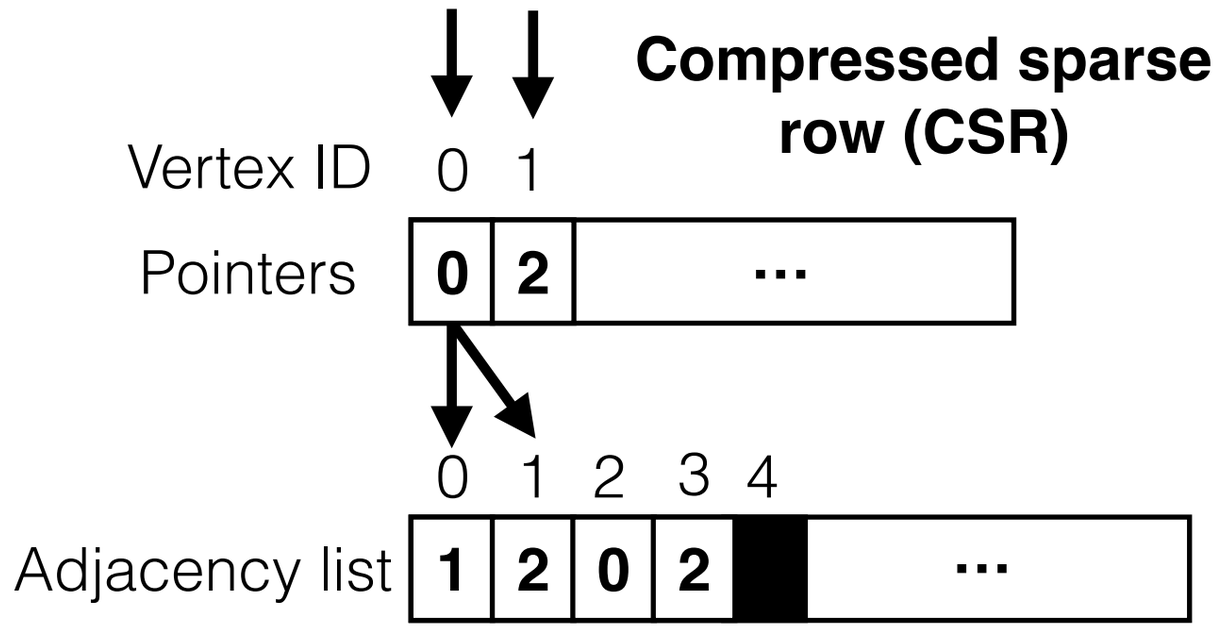

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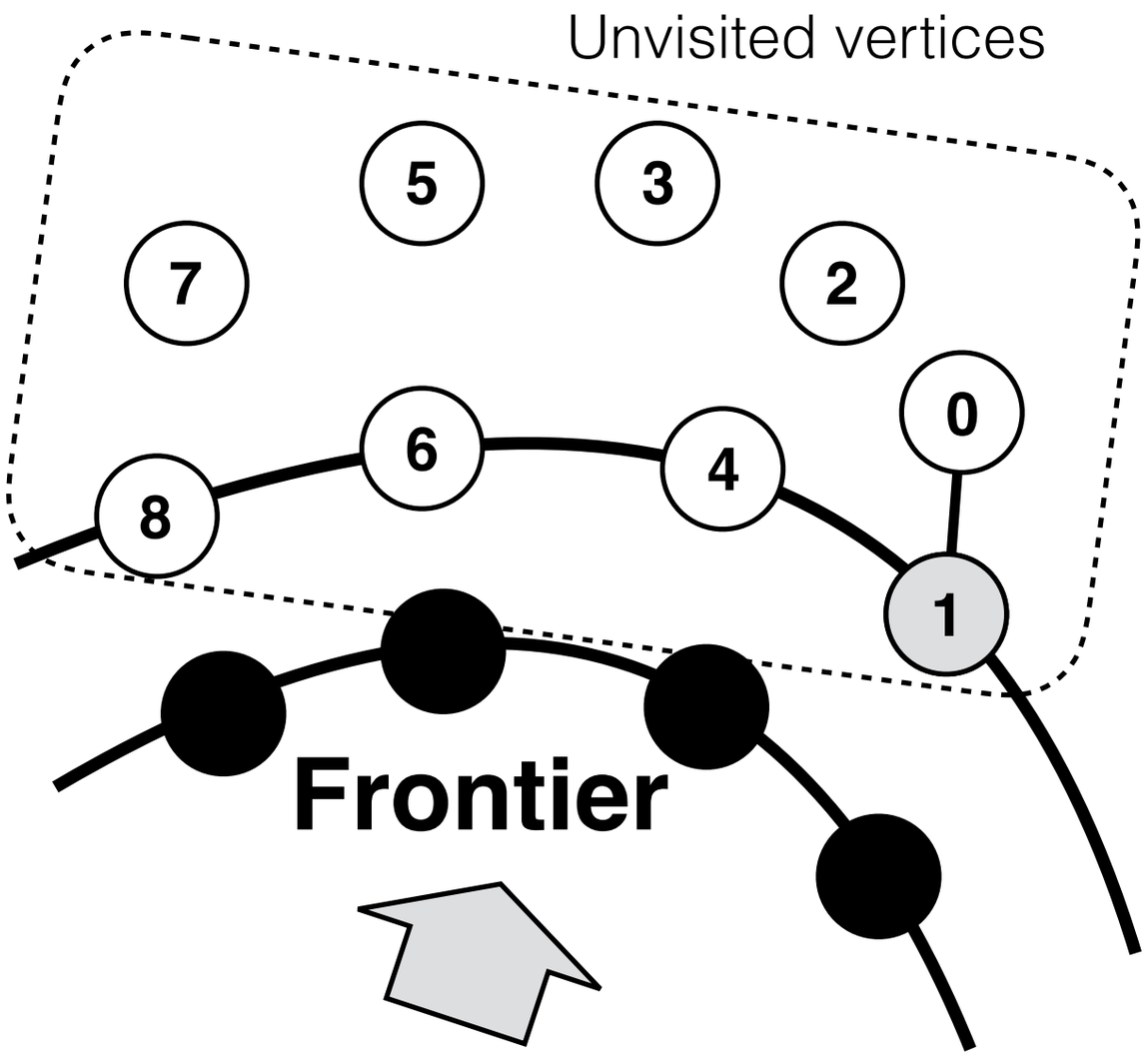

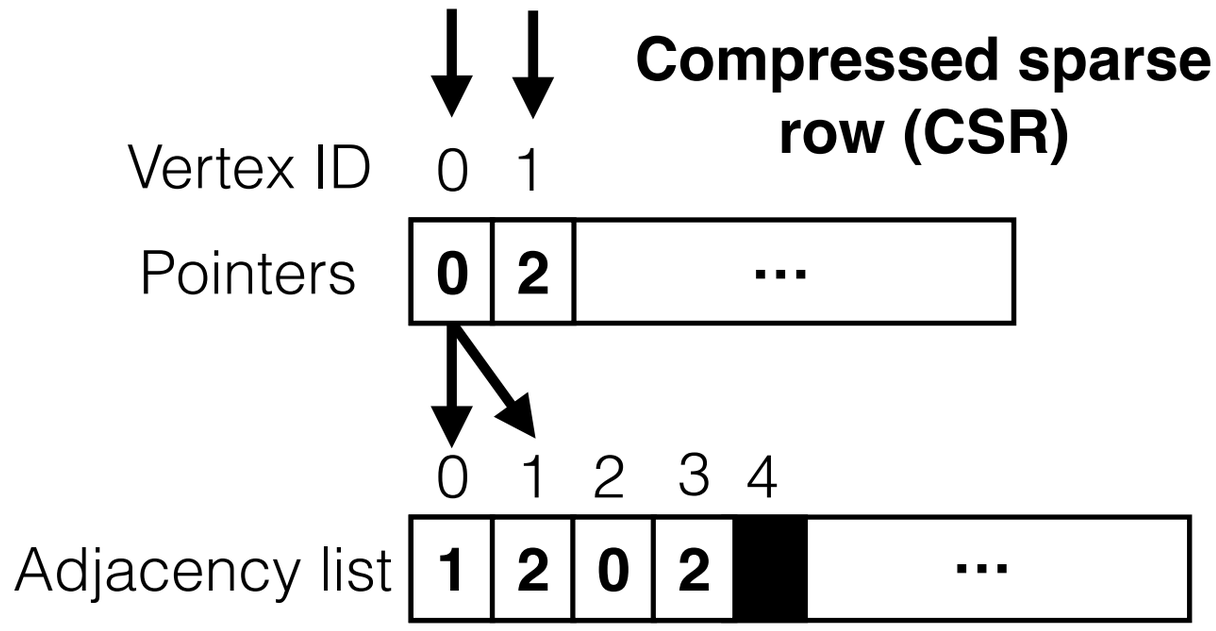

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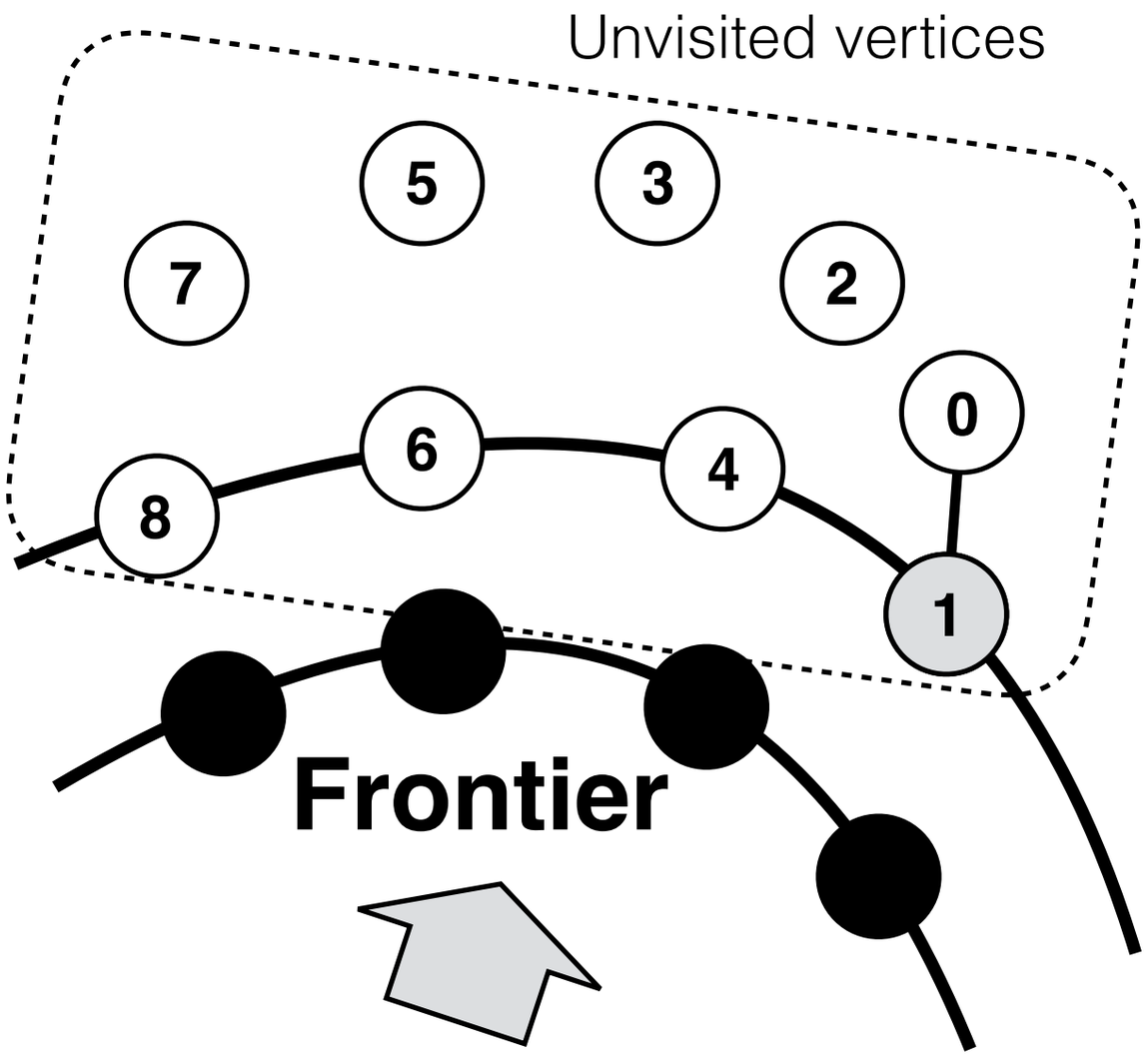

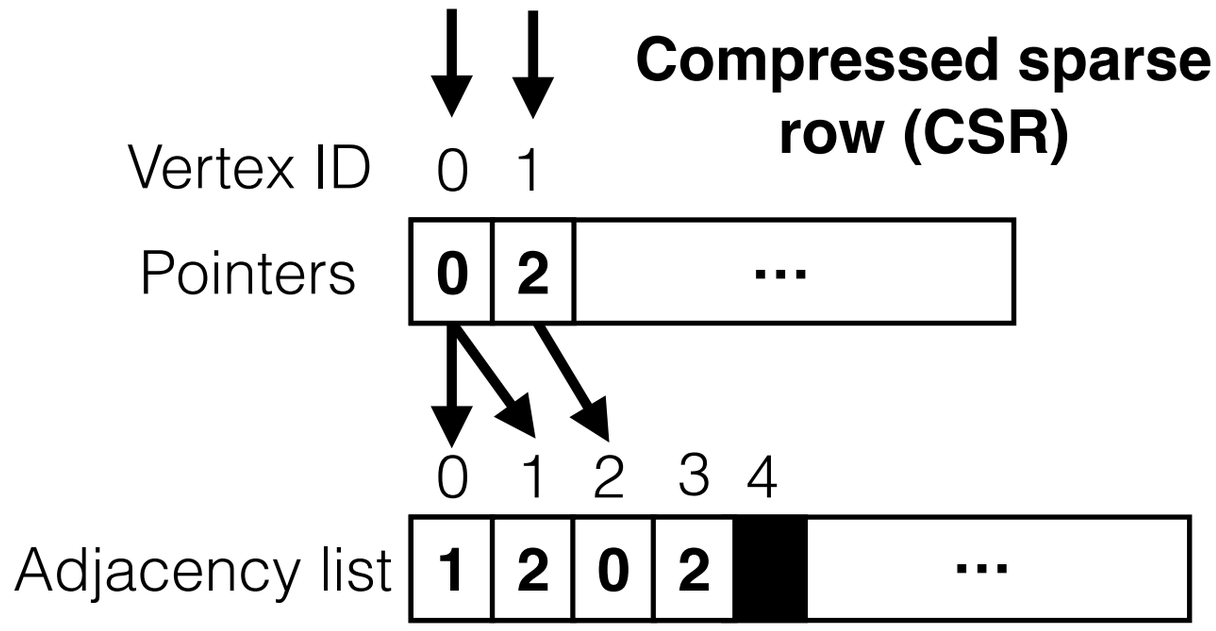

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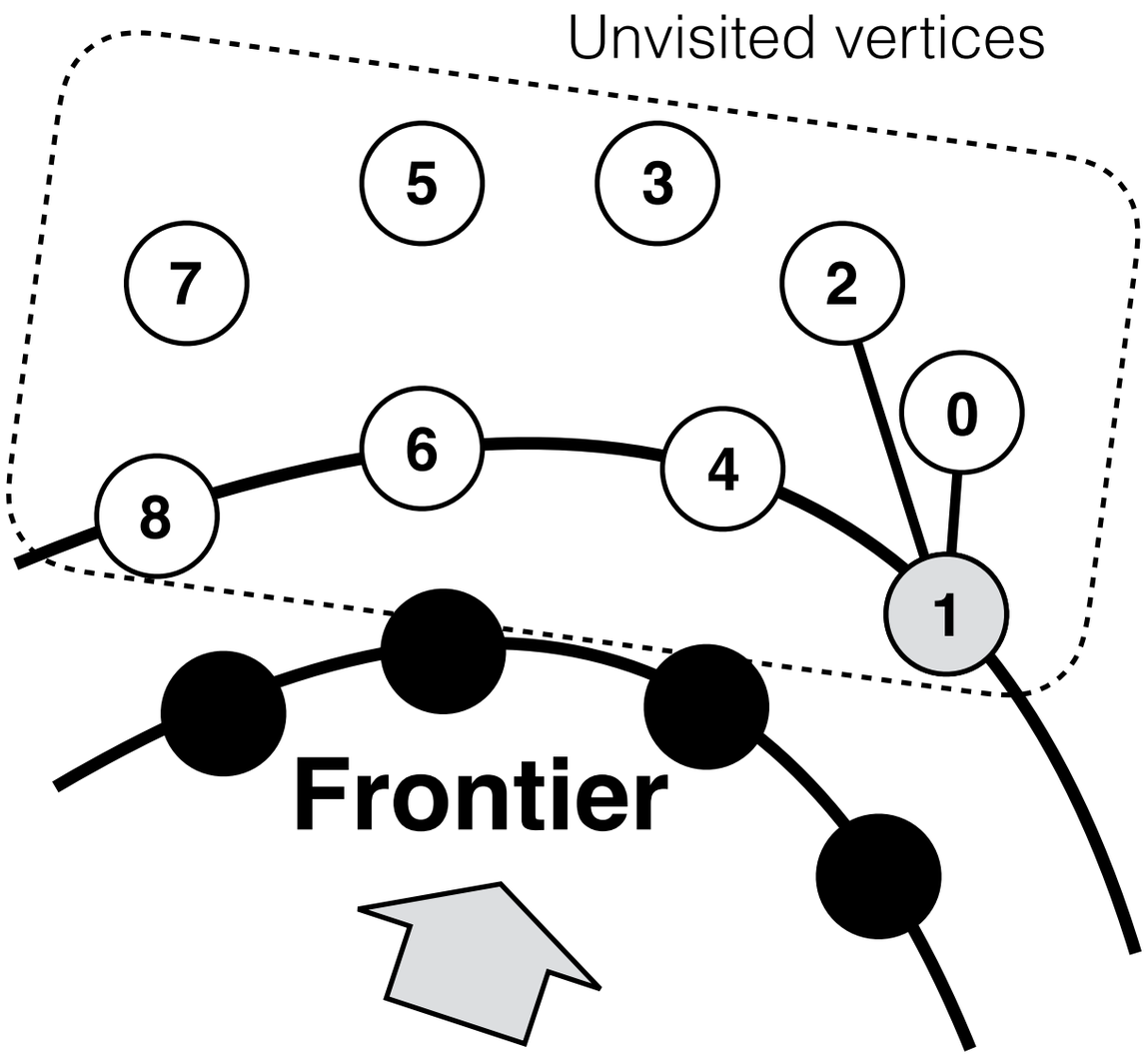

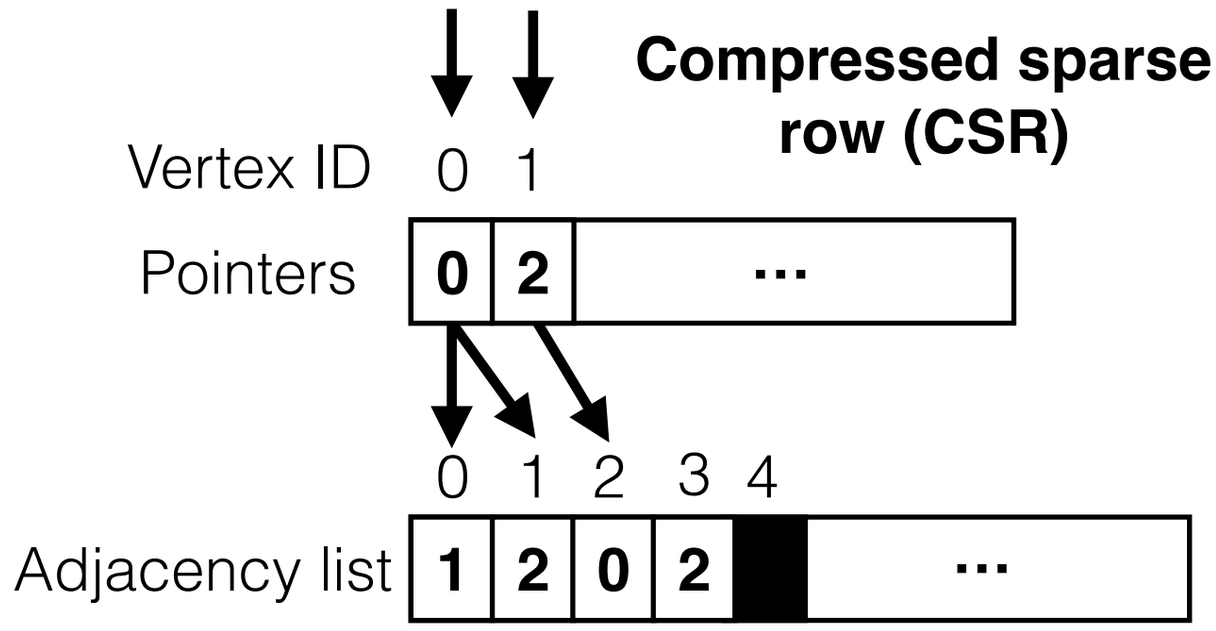

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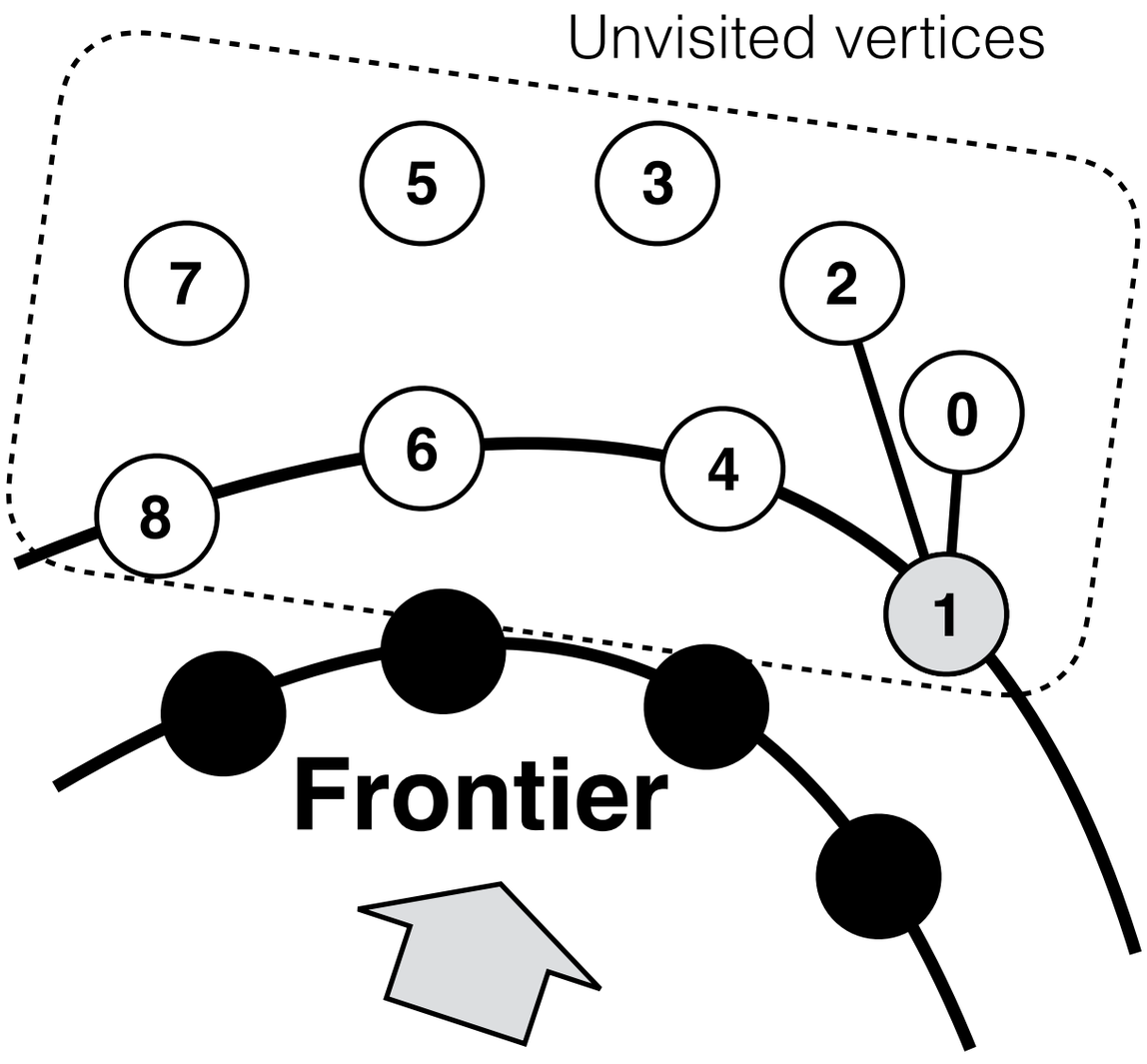

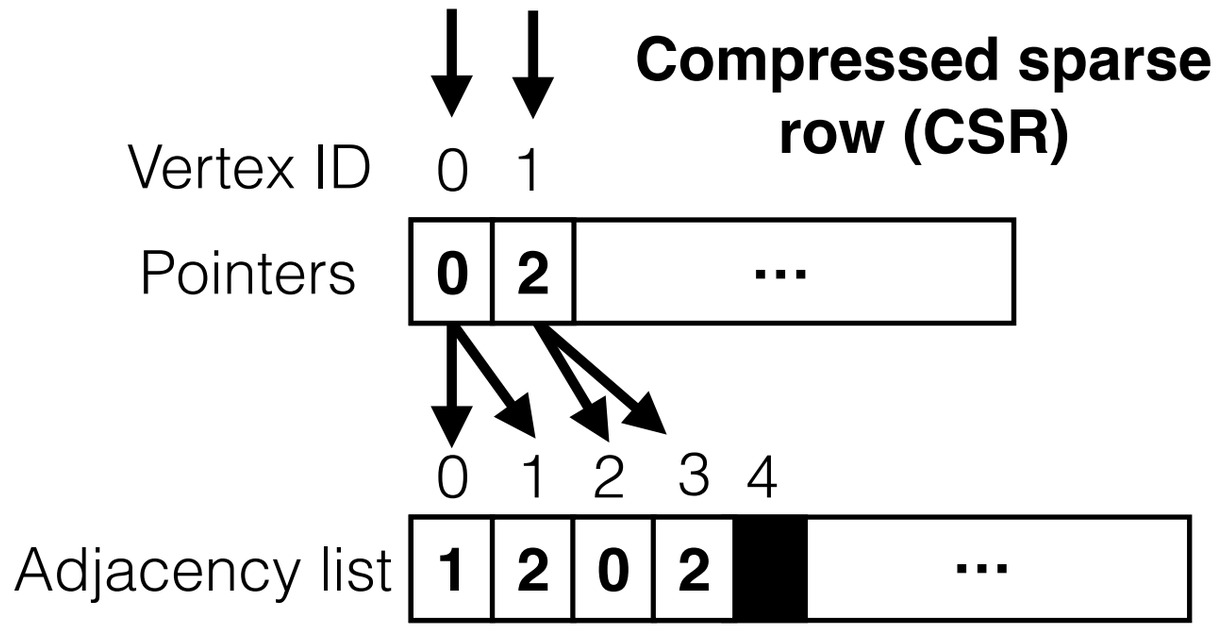

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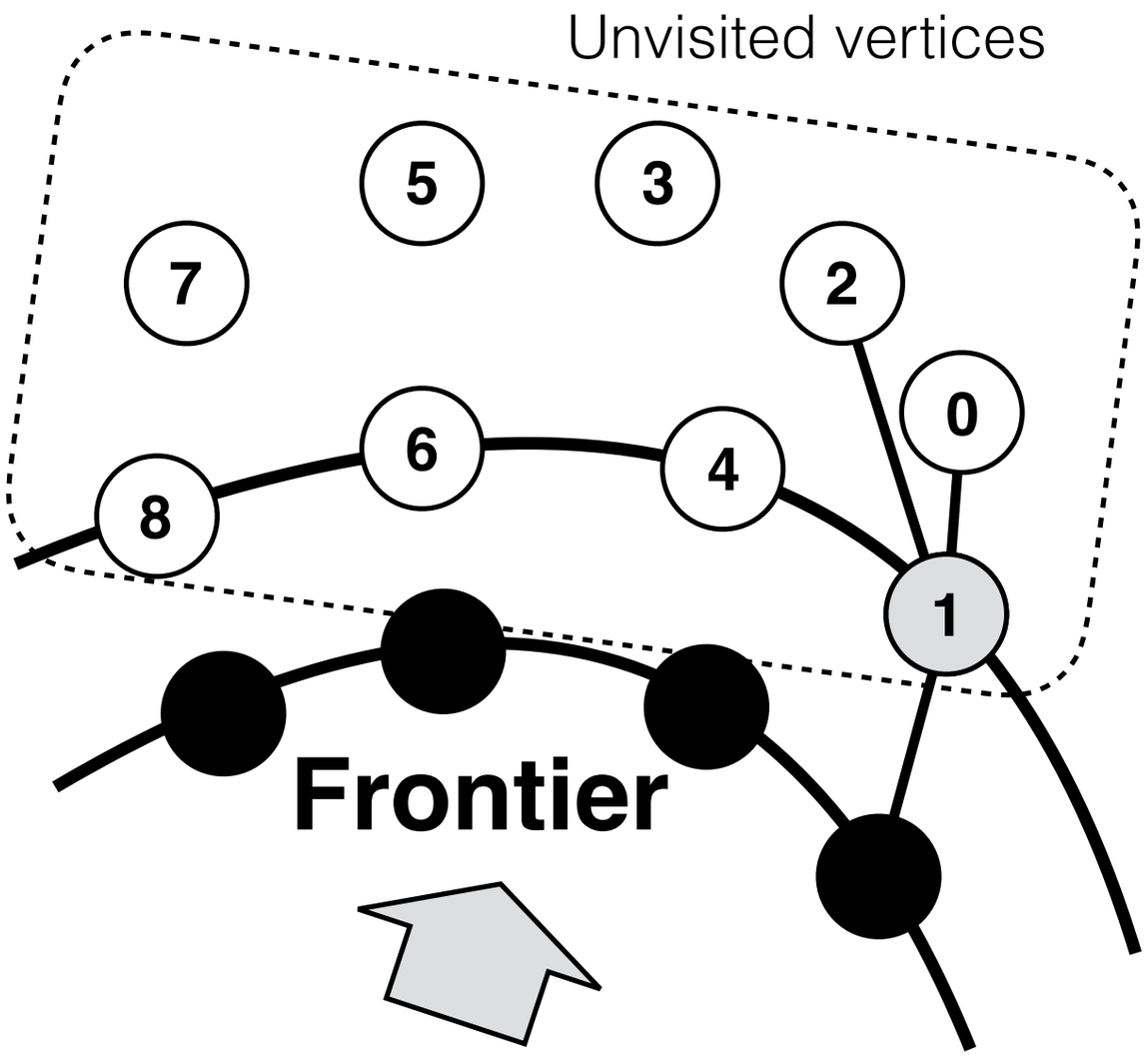

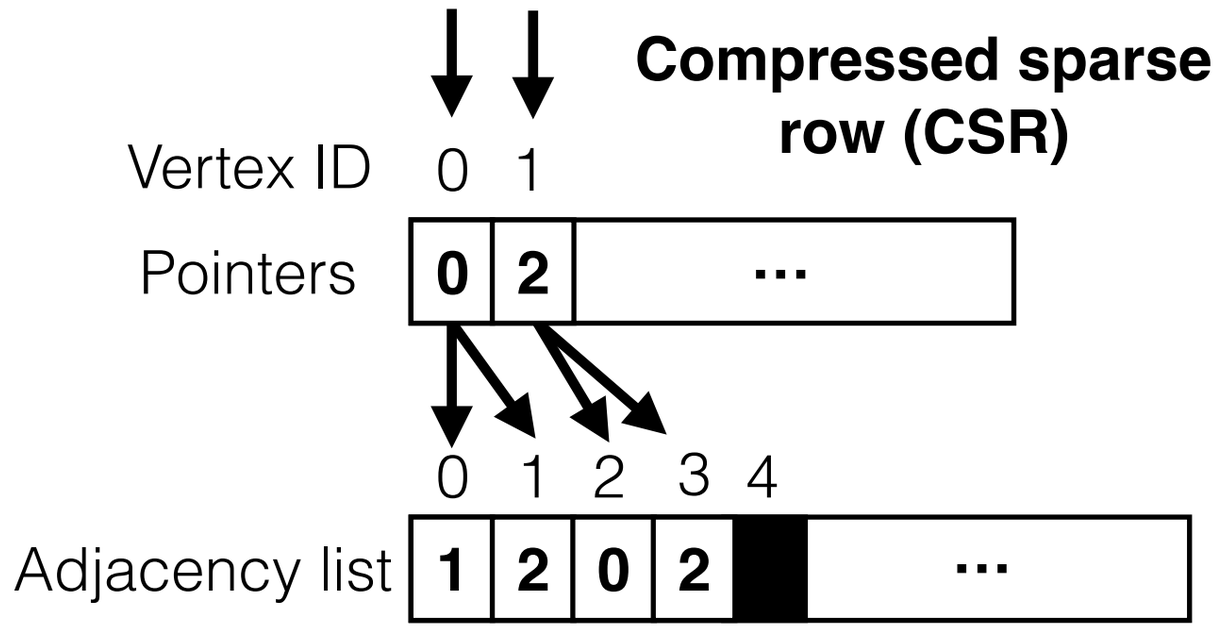

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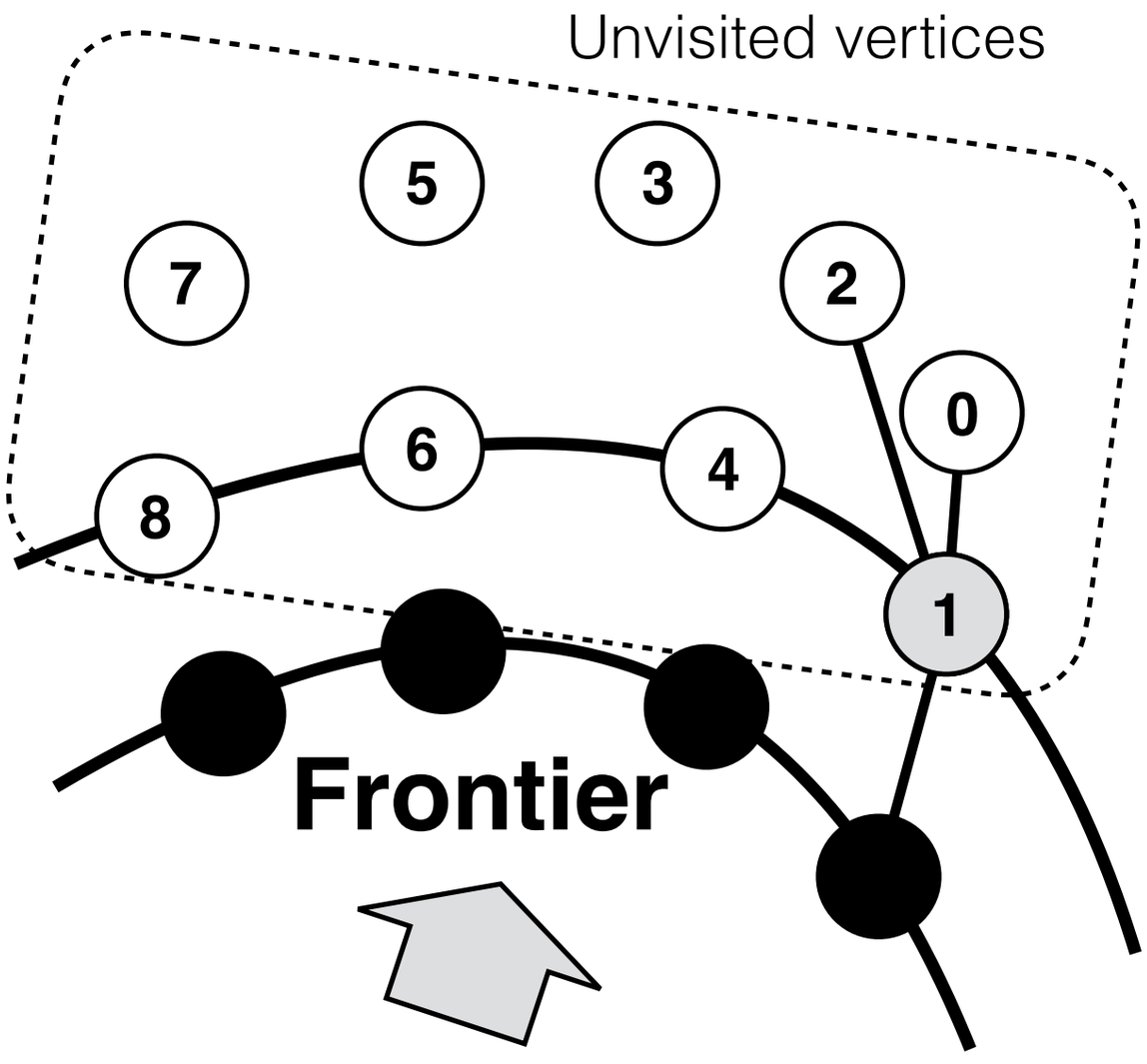

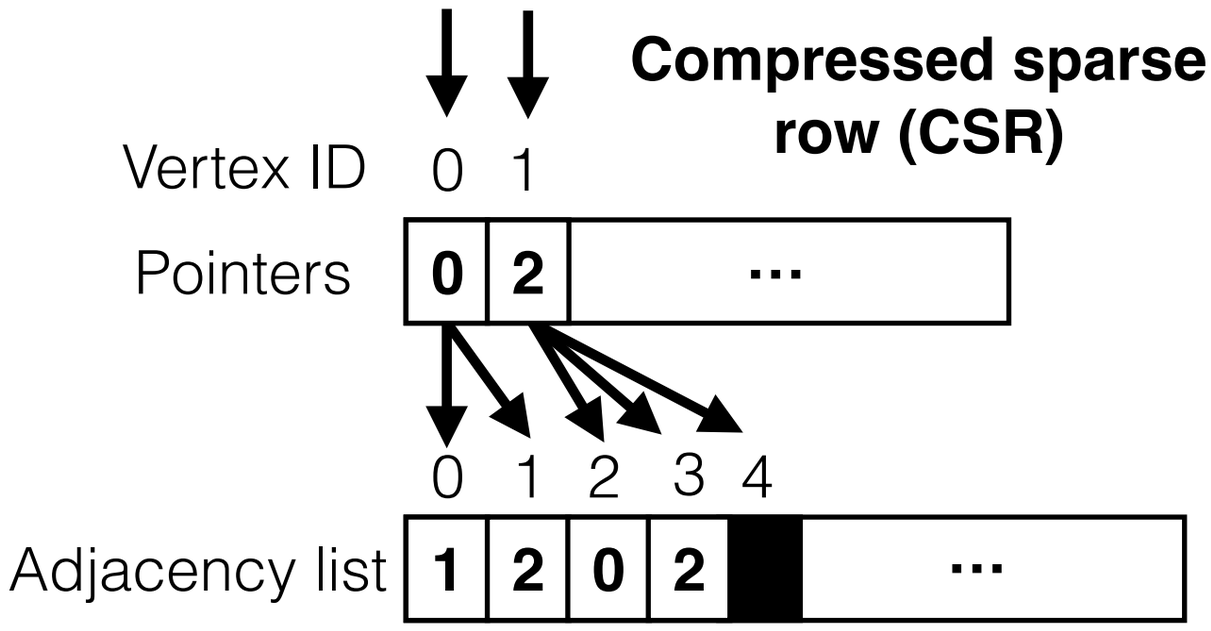

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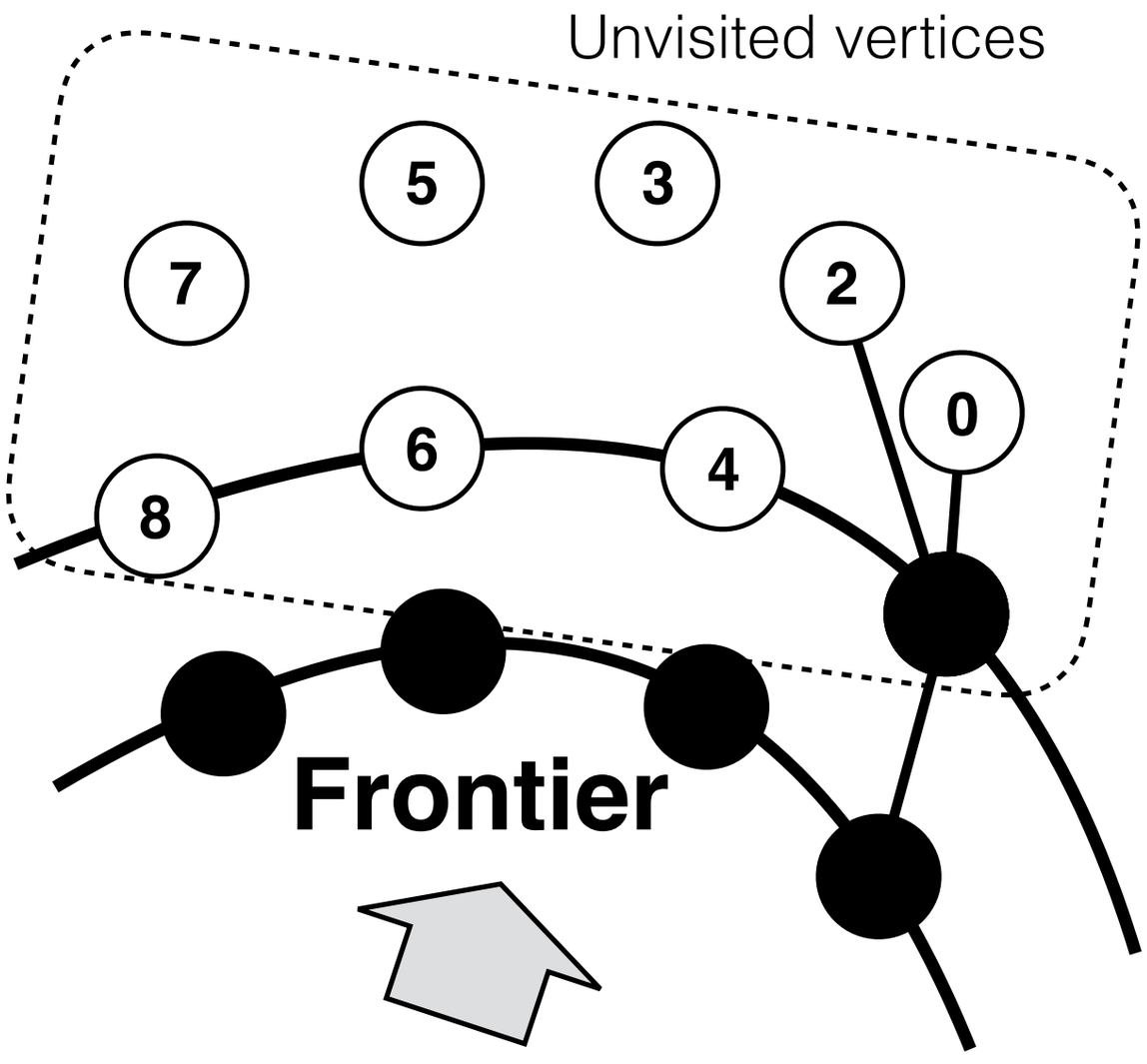

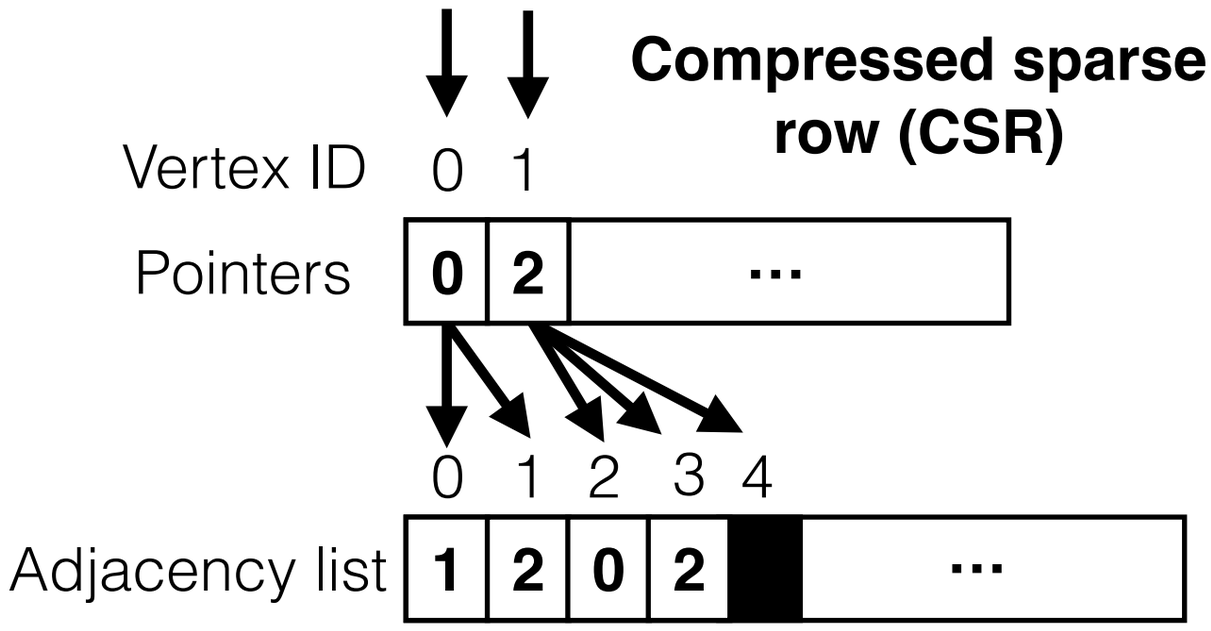

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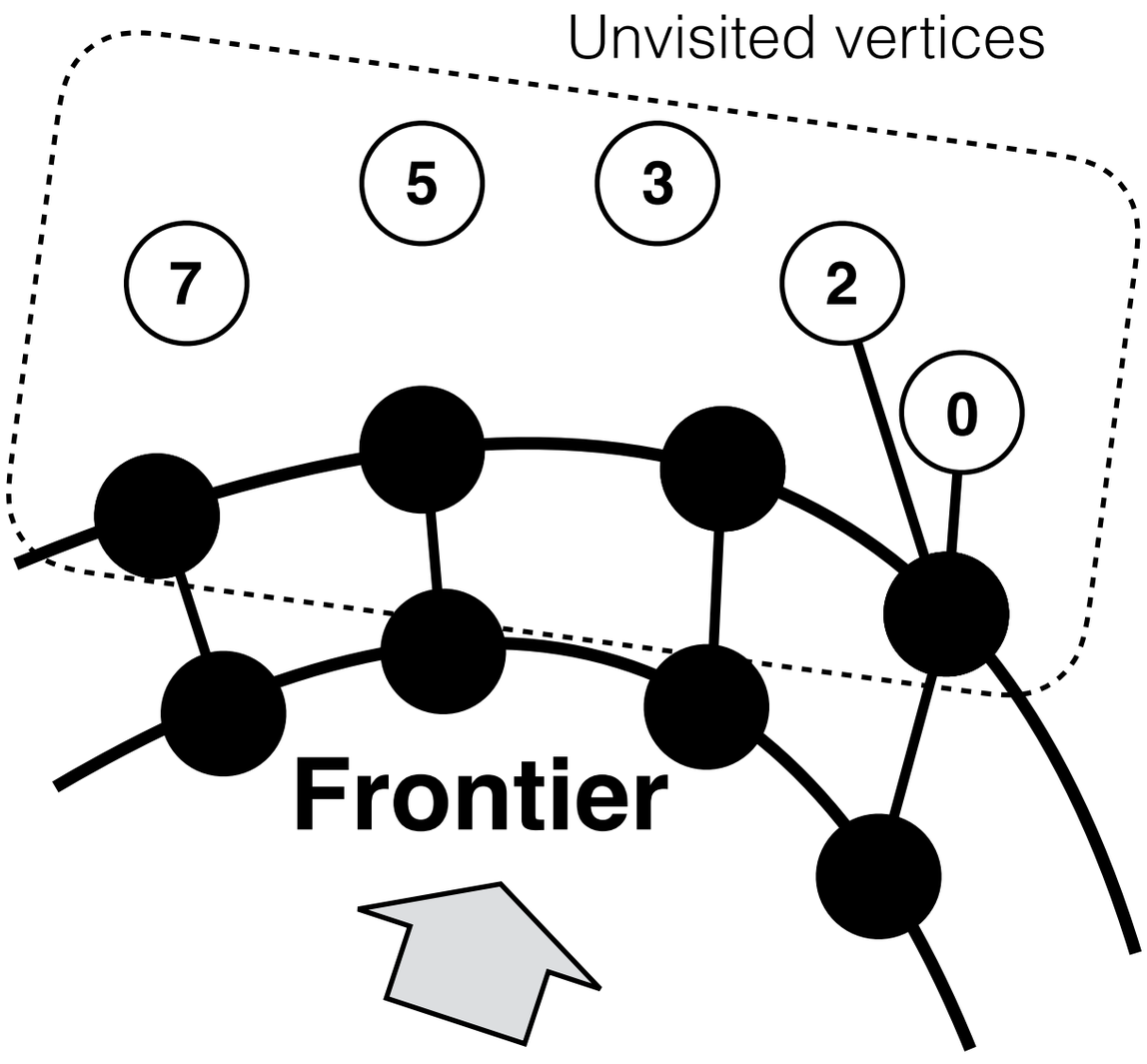

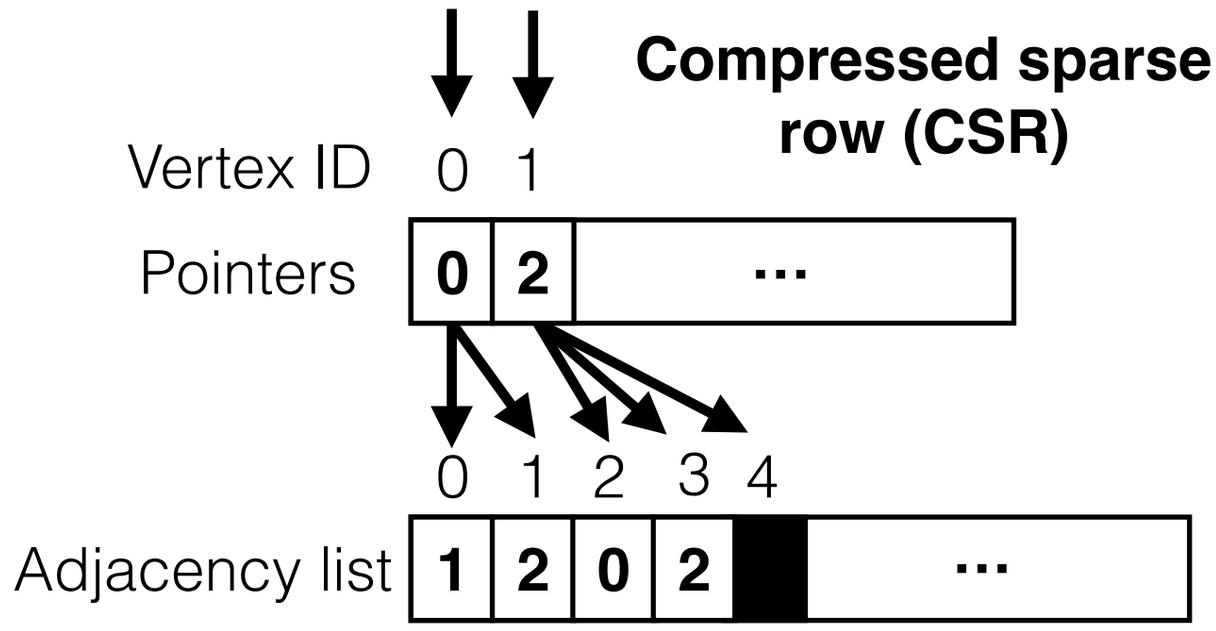

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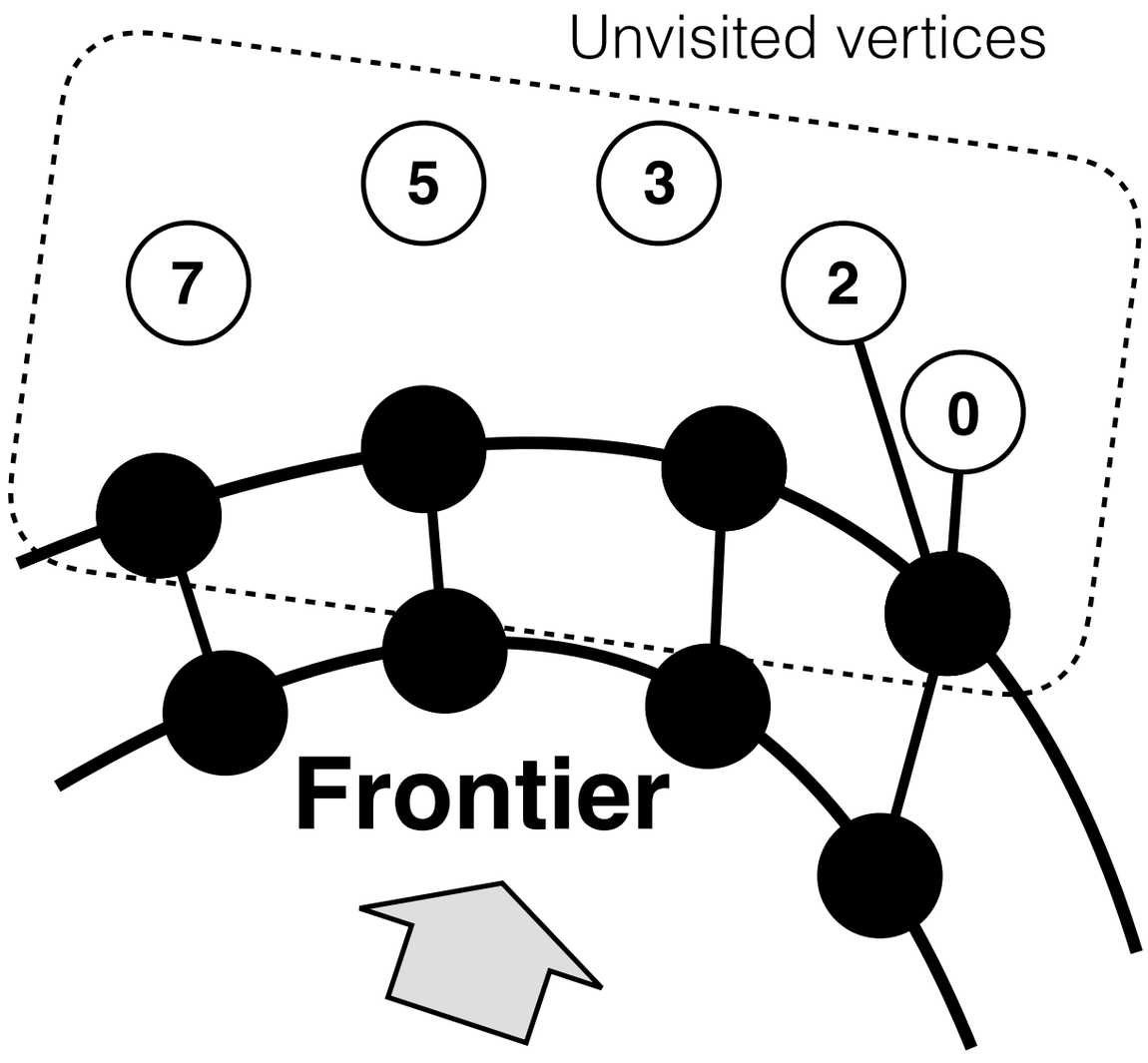

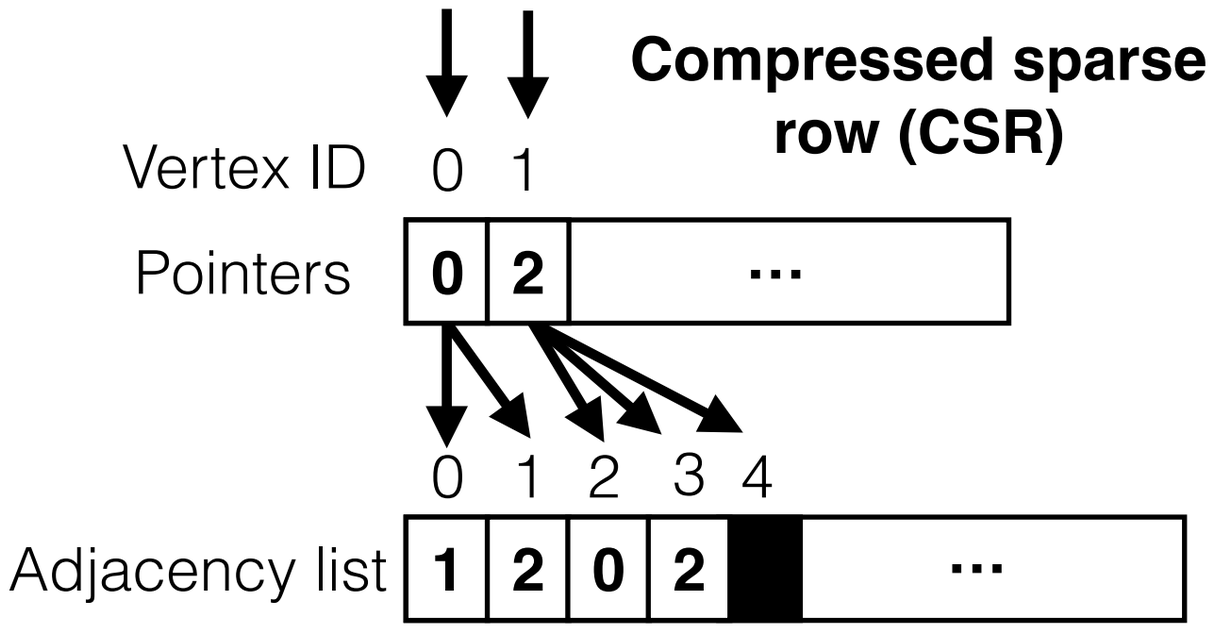

- This search is parallelized using OpenMP
- Memory-intensive

Agenda

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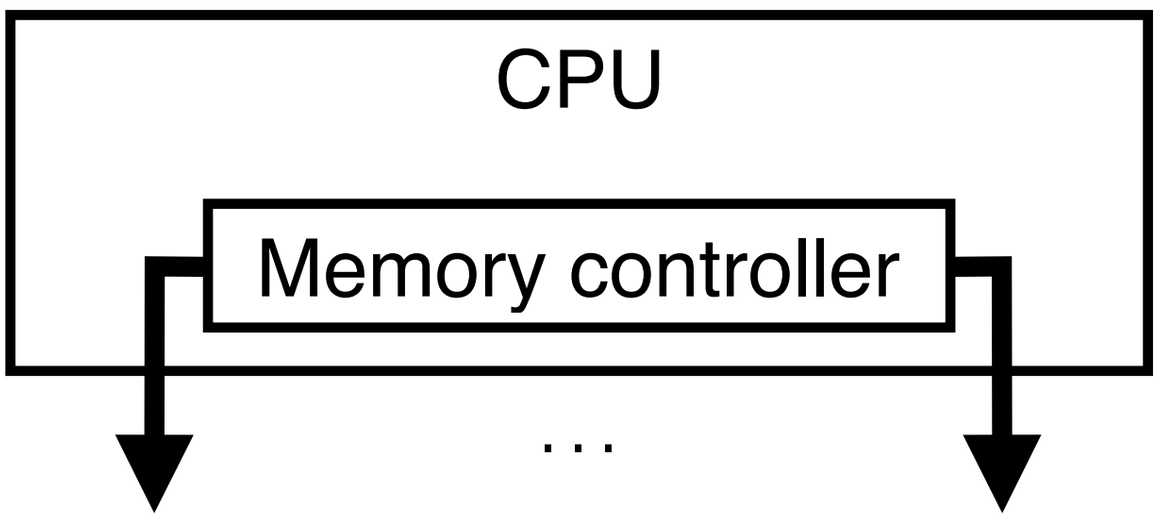
Multibank architecture



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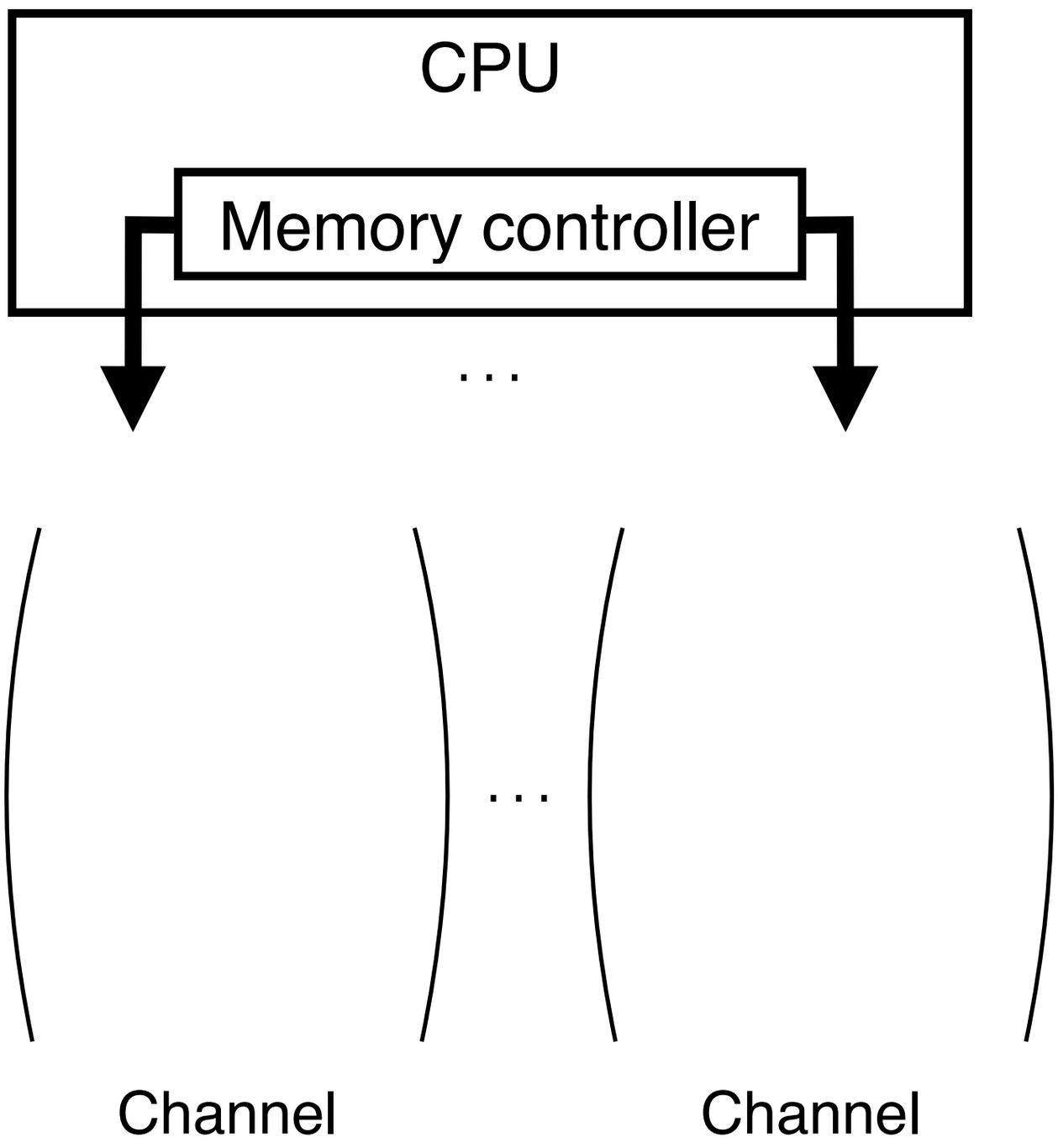

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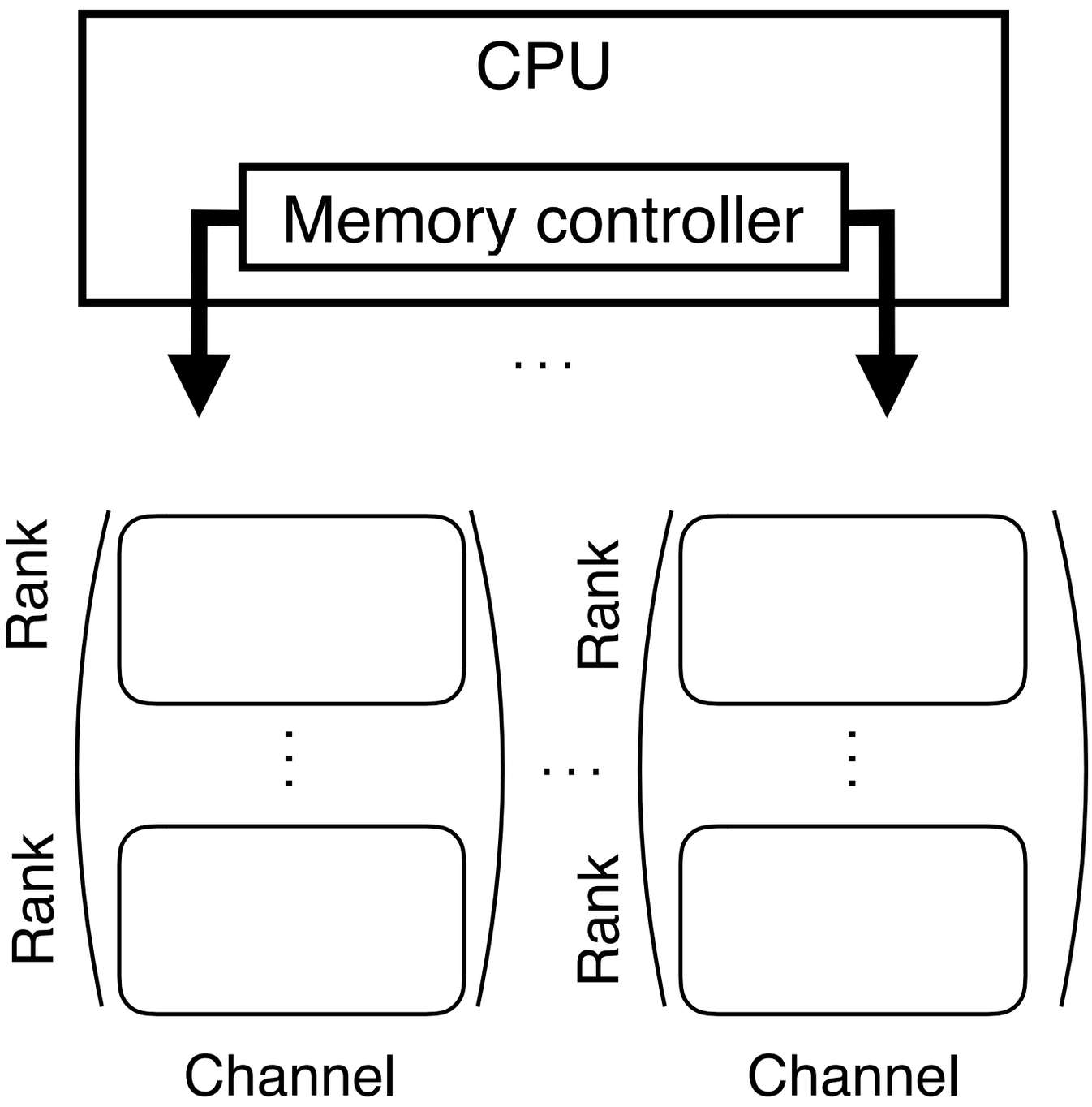

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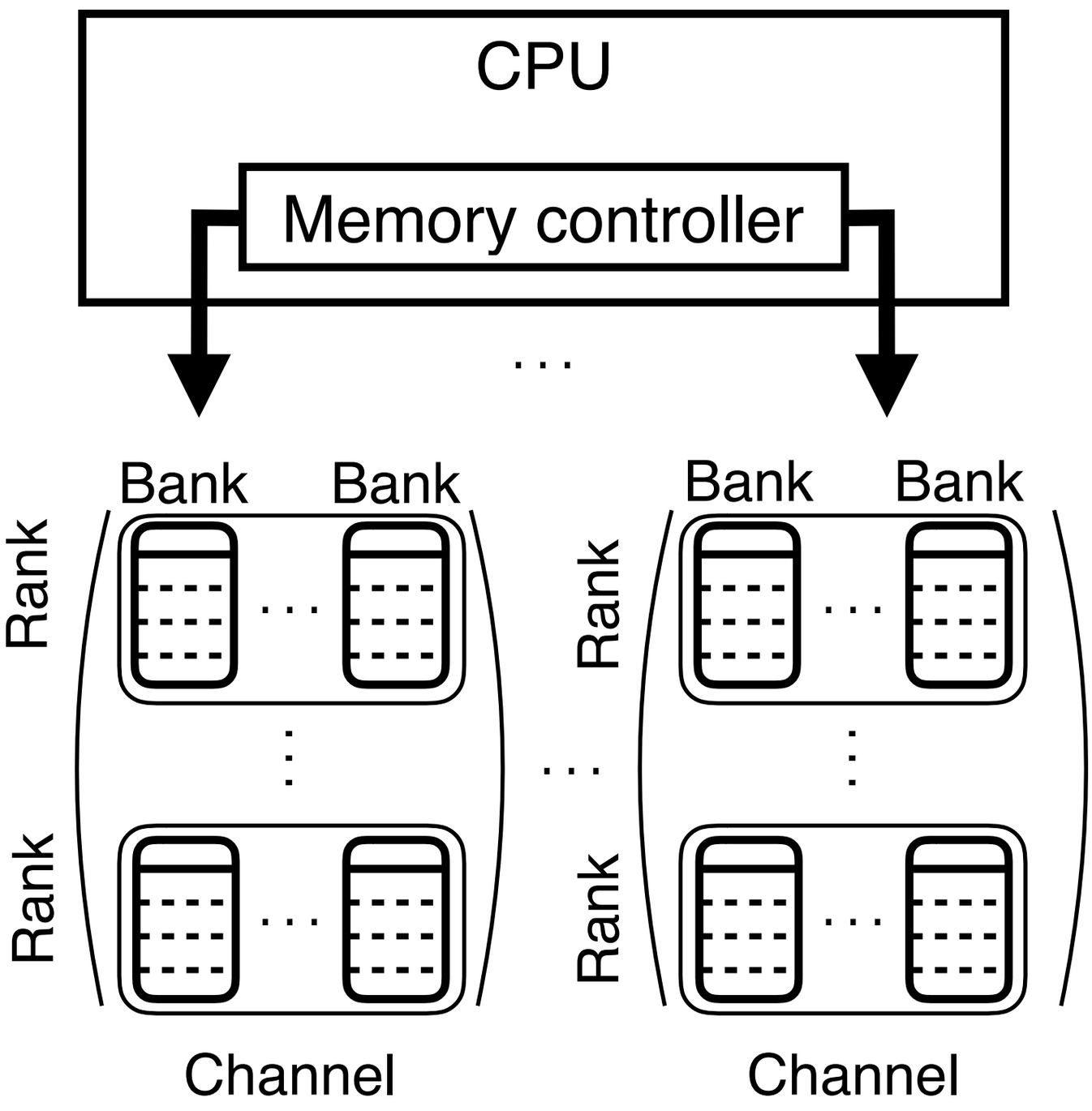

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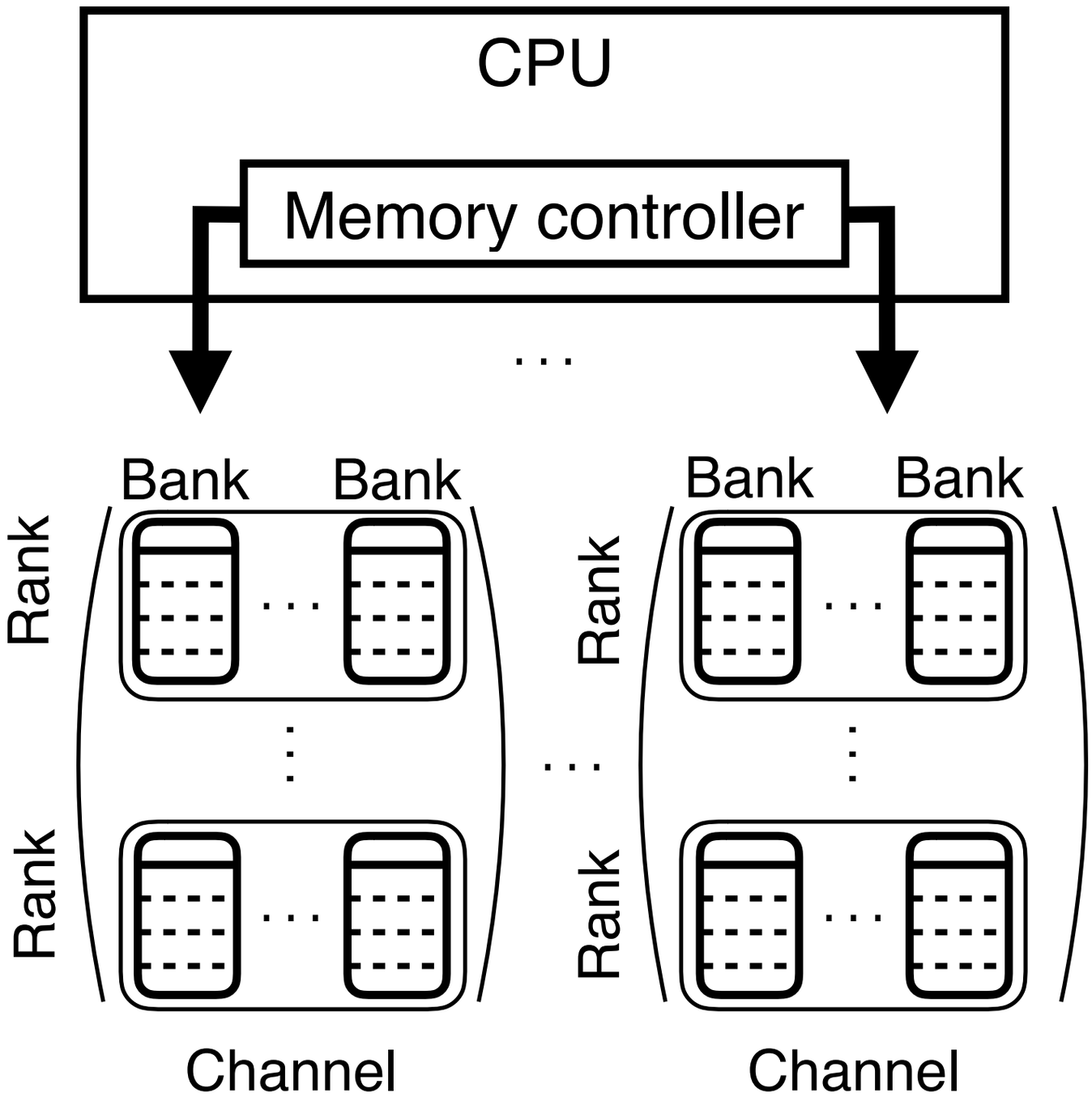

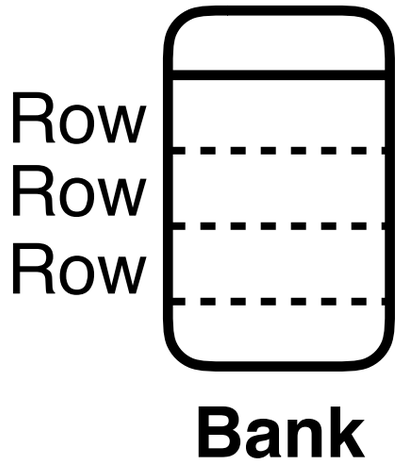

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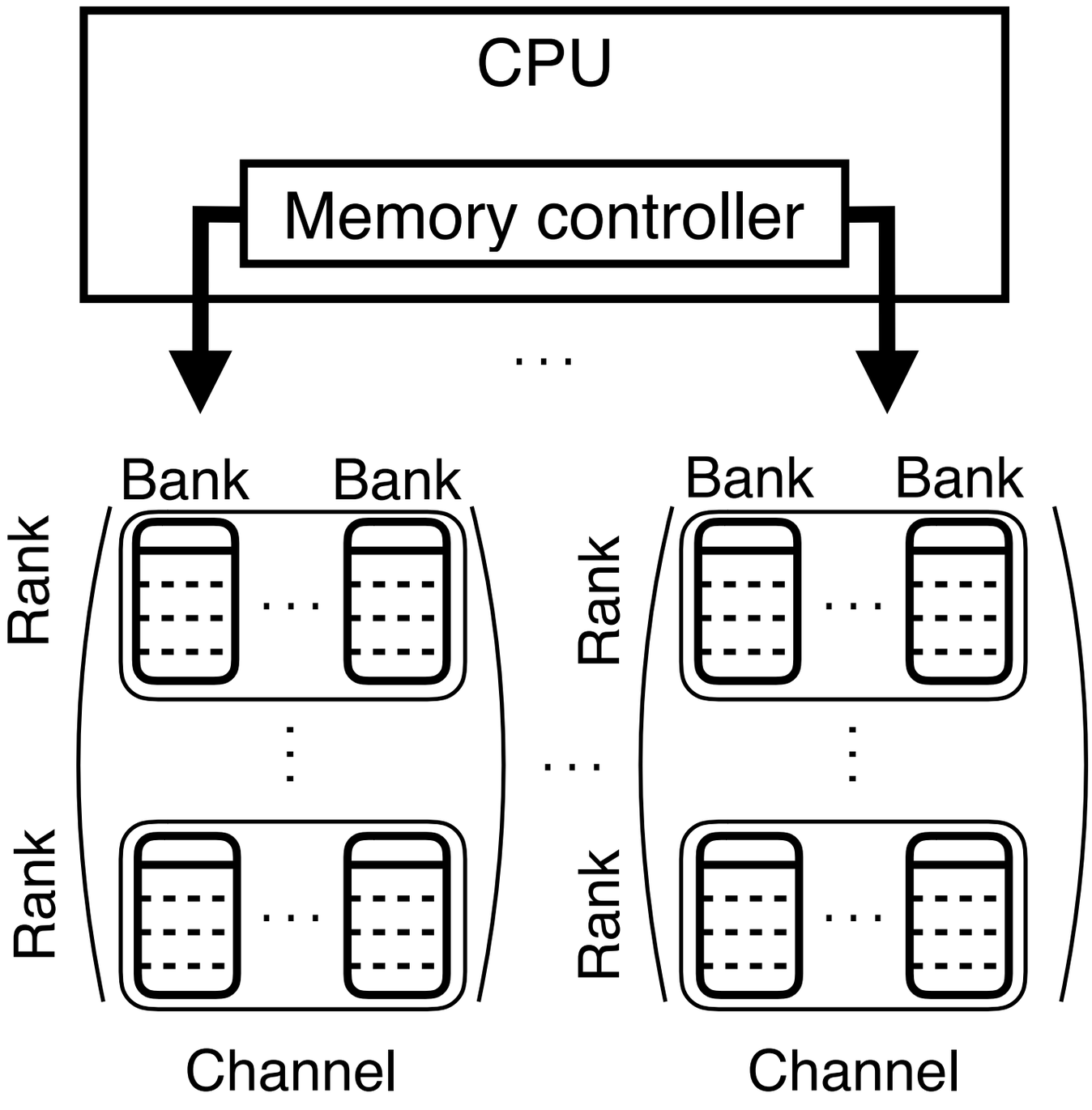

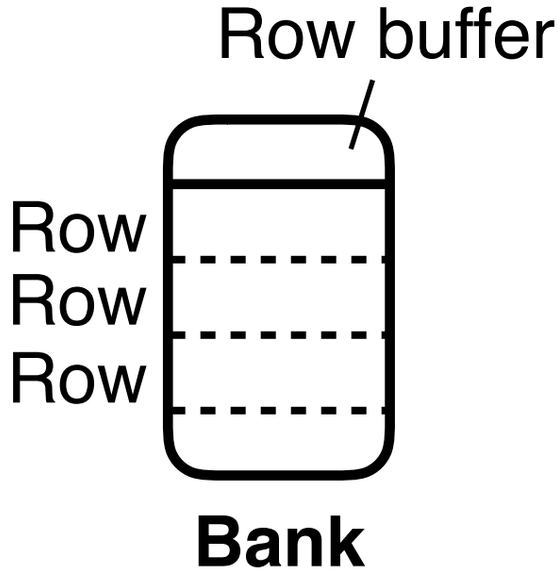

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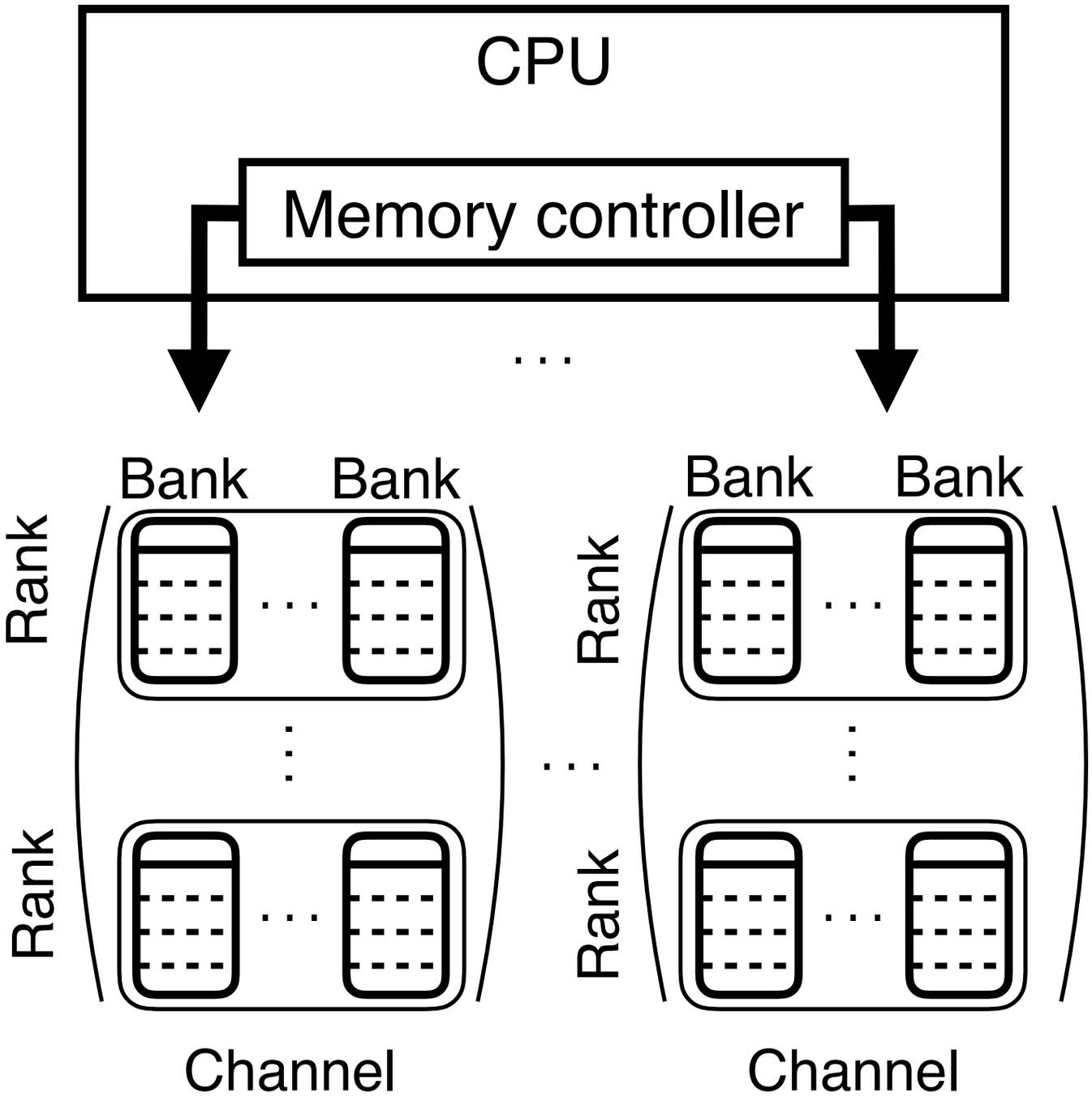

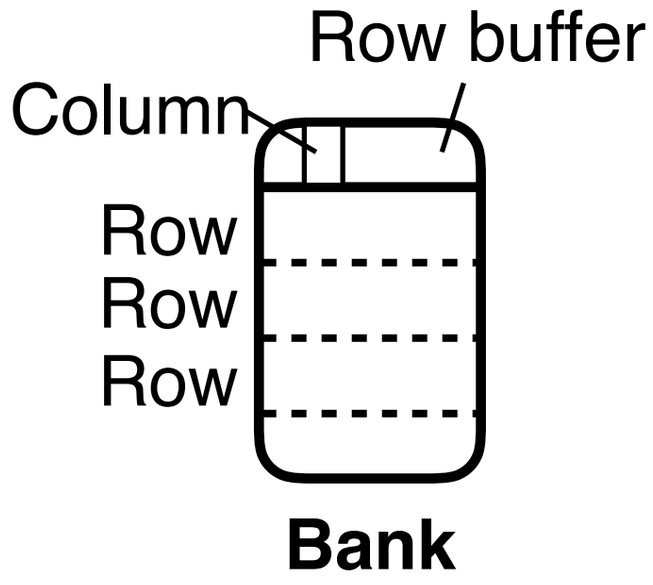

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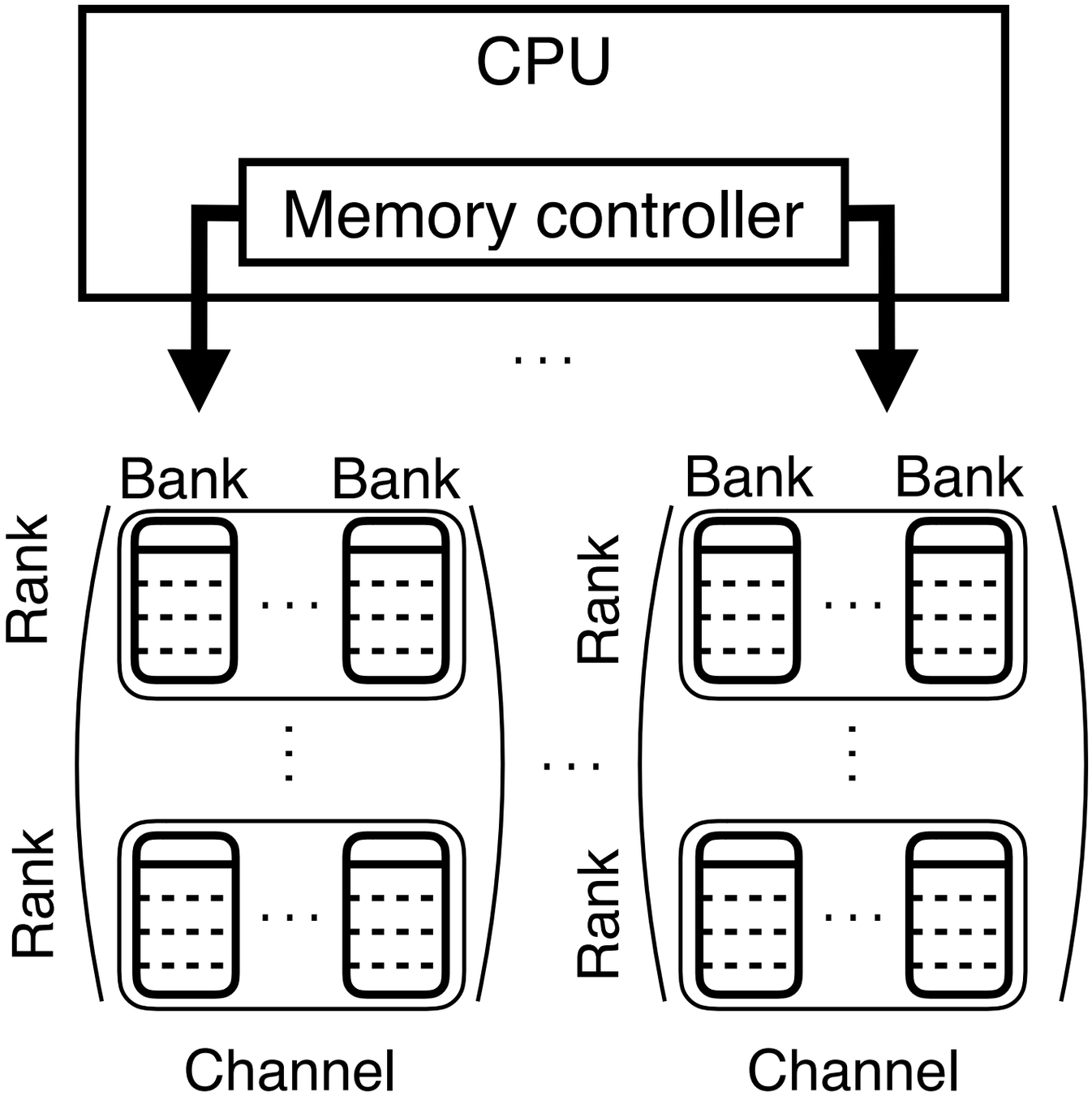
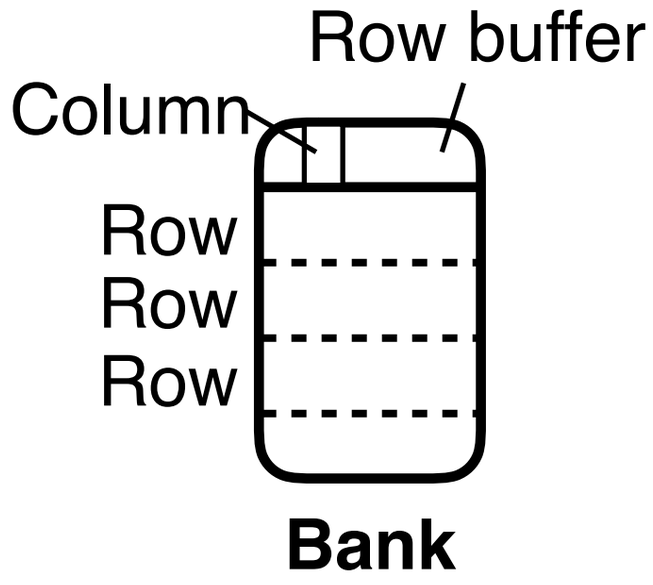
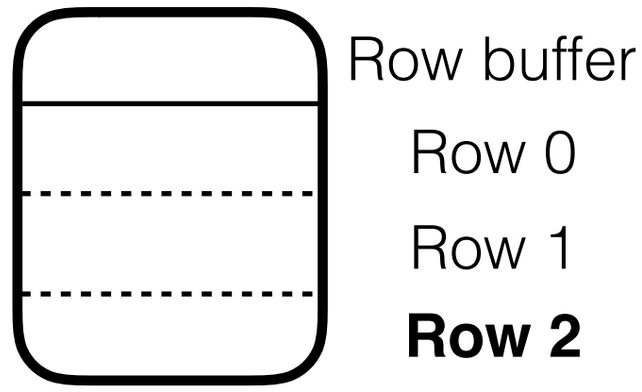




Multiple banks can be accessed in parallel
→ ***bank parallelism***

Three Types of Row Buffer Accesses



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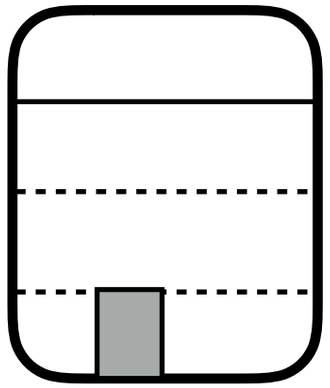

Access to data in **row 2**

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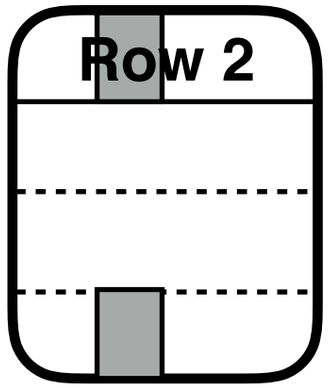

Row buffer

Row 0

Row 1

Row 2

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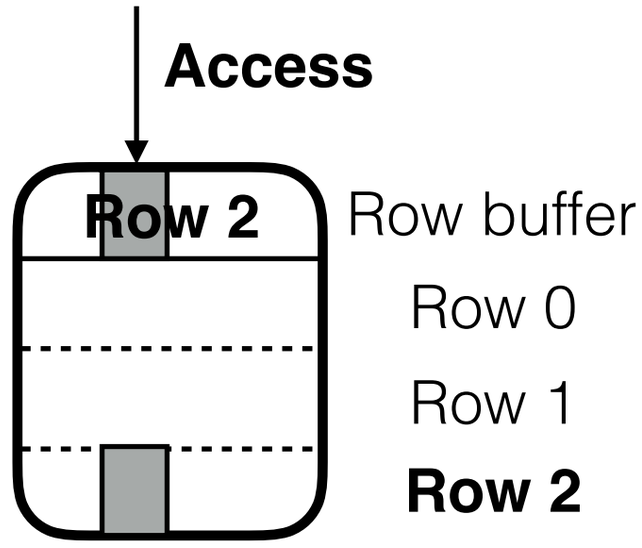

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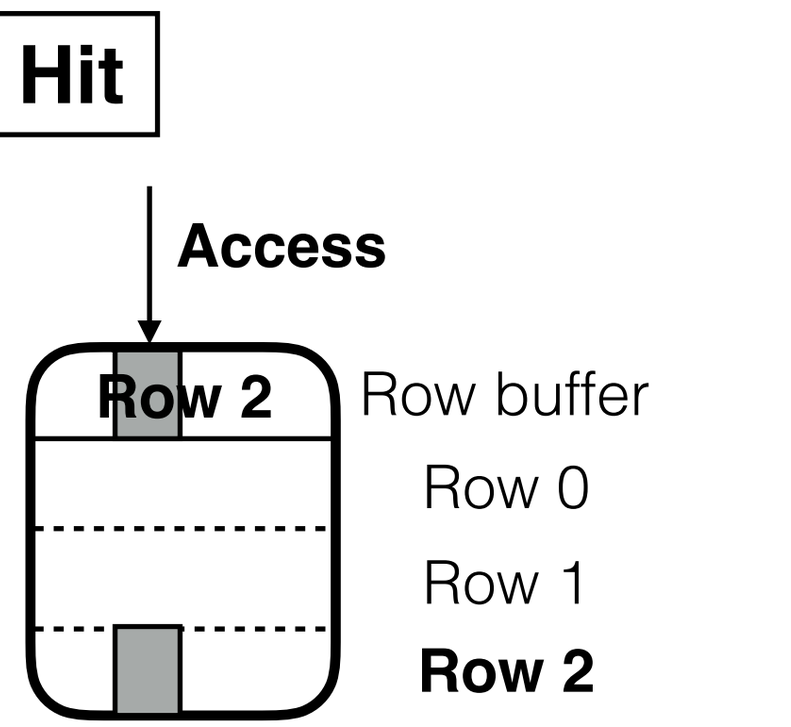

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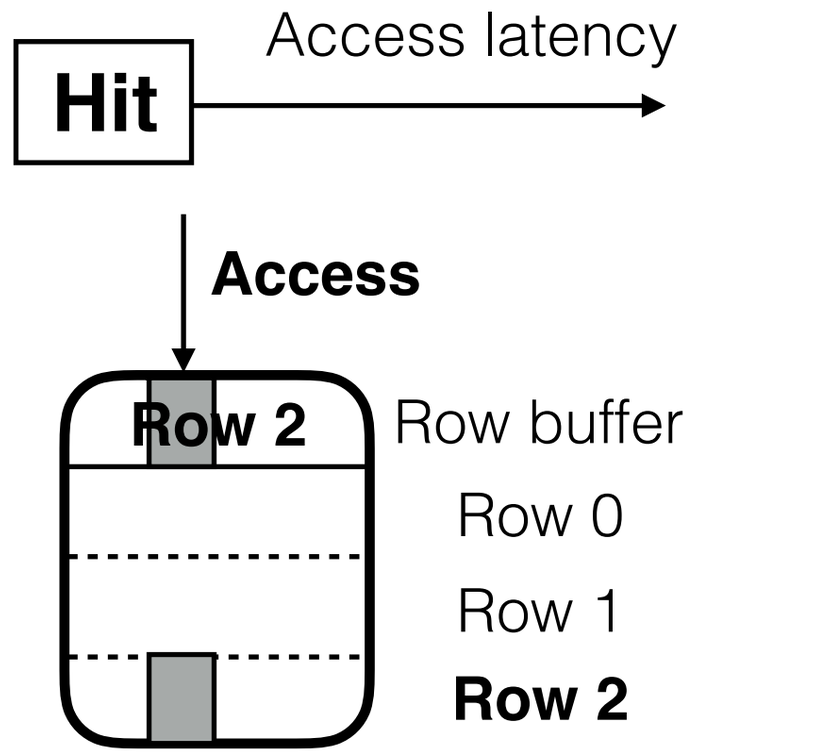

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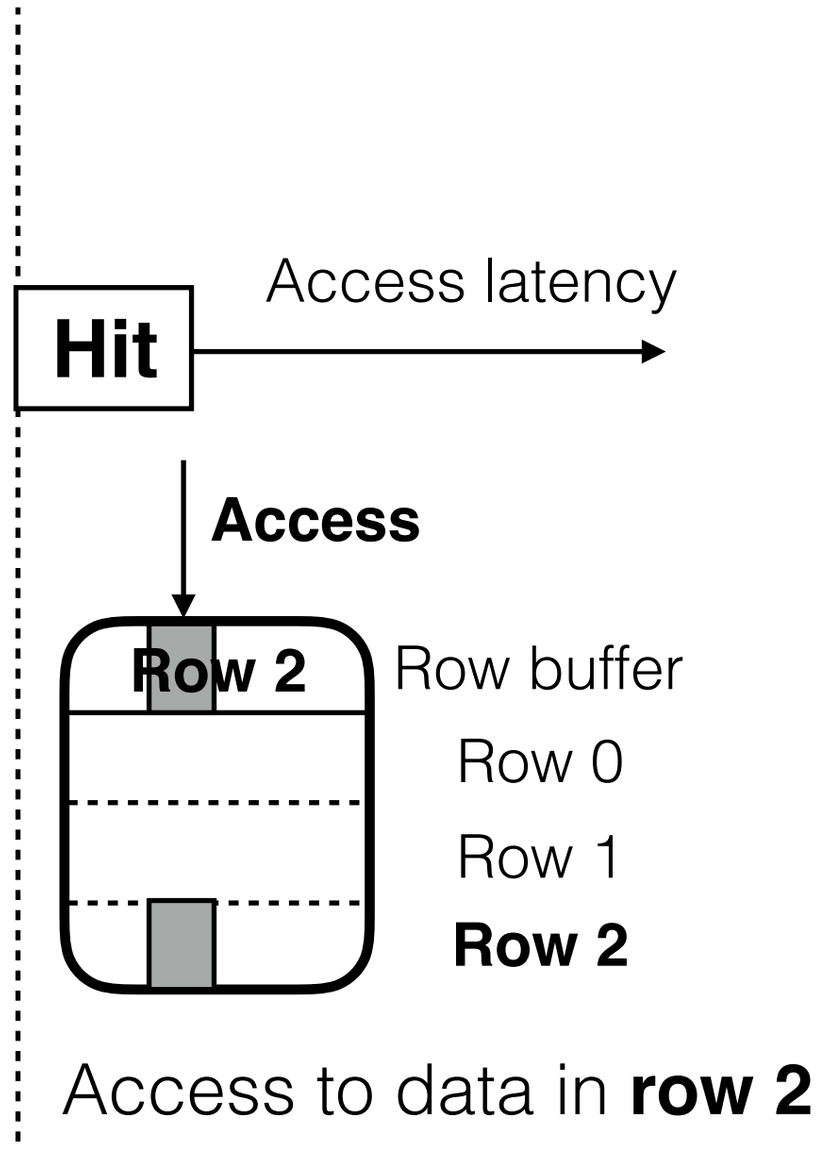

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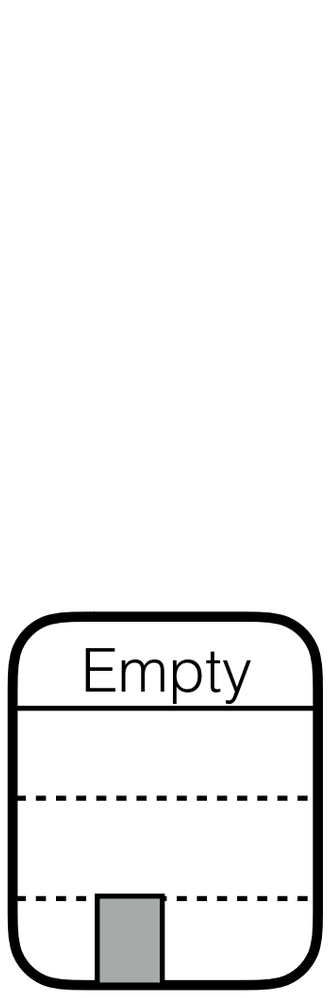

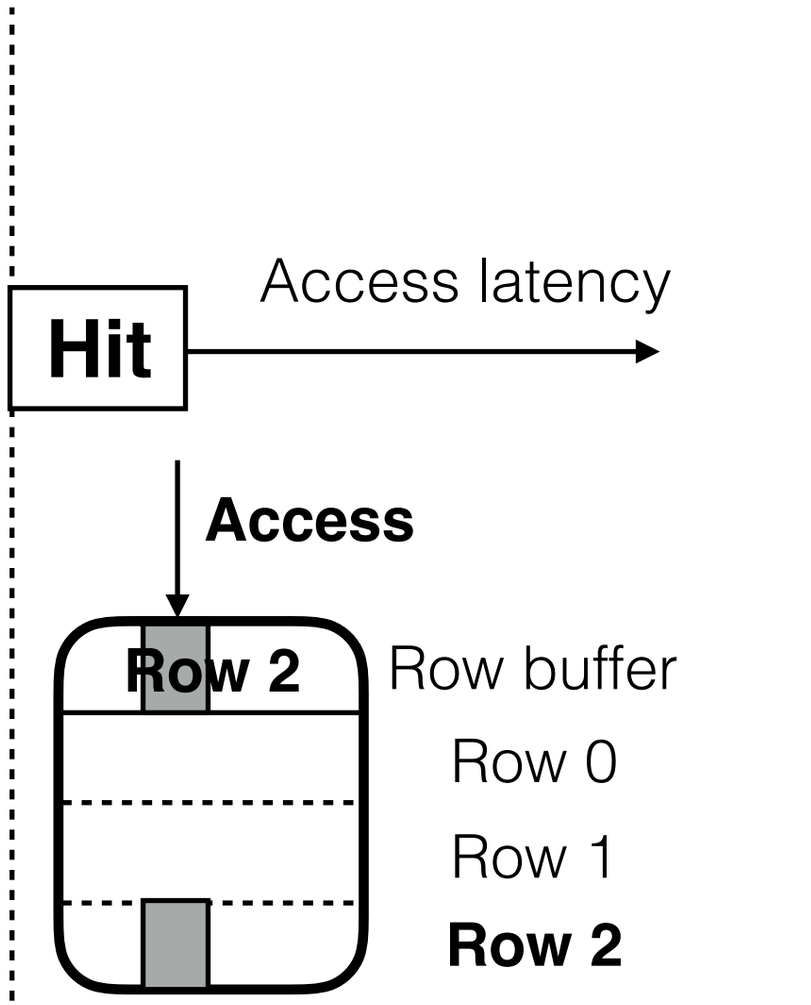

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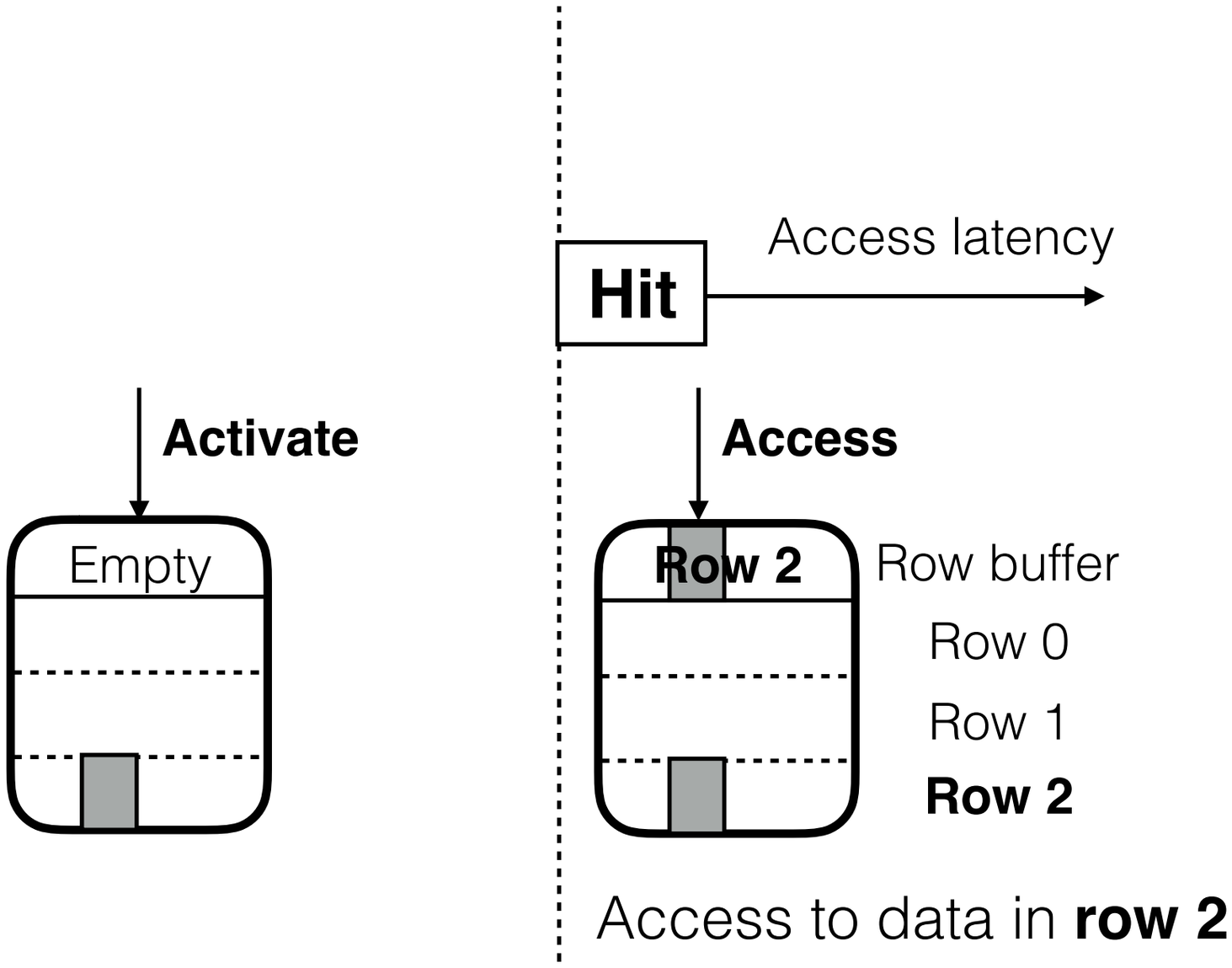

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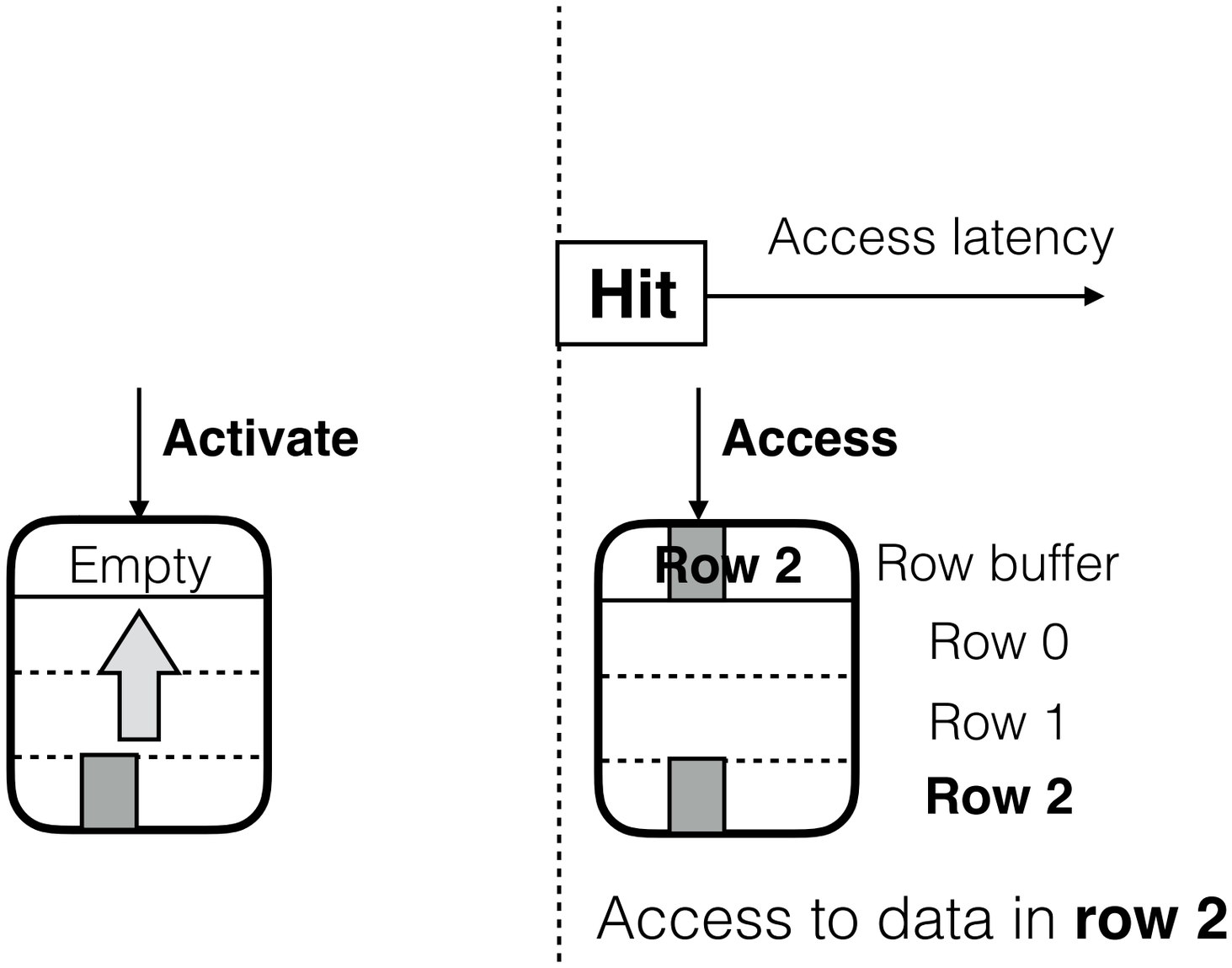

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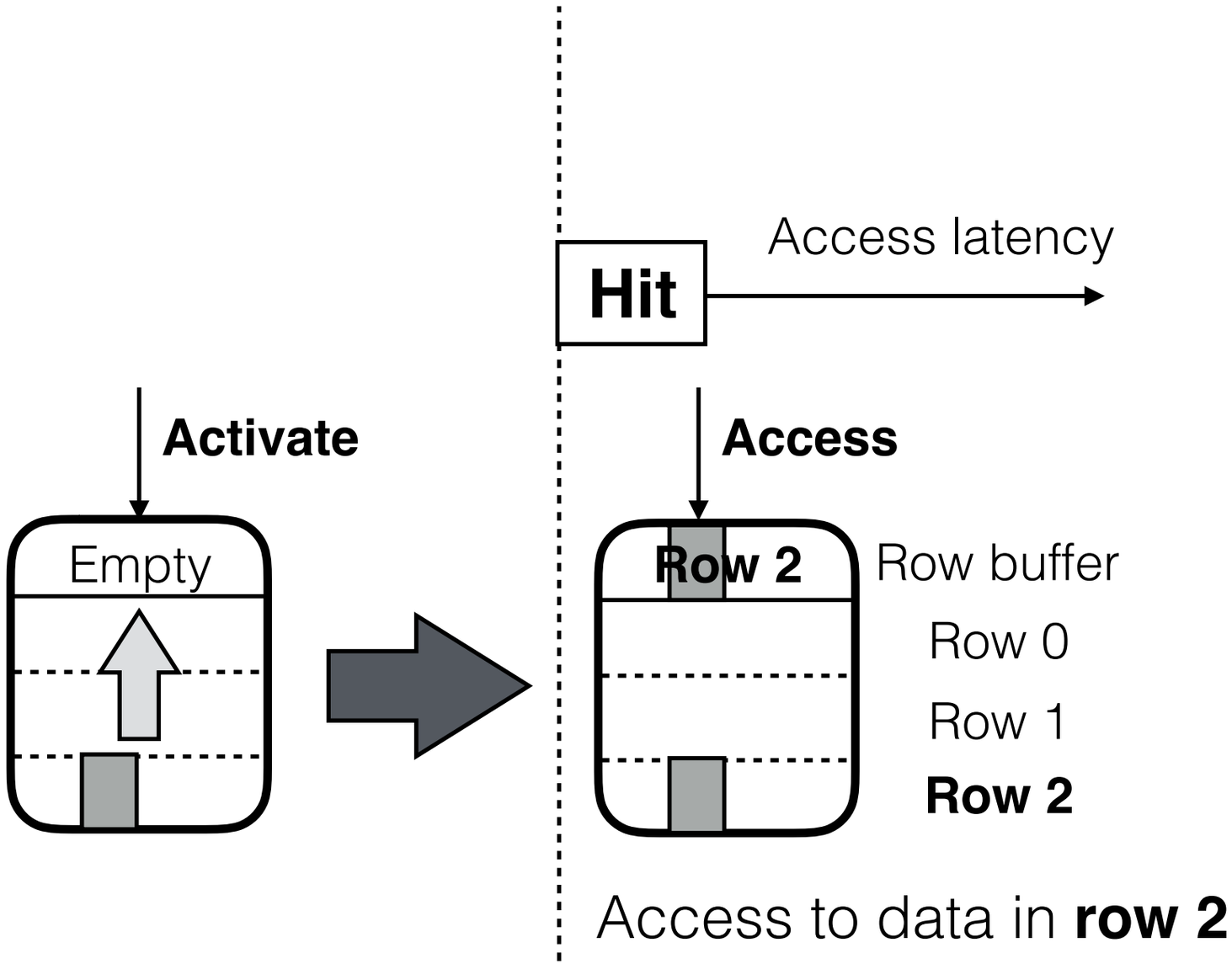

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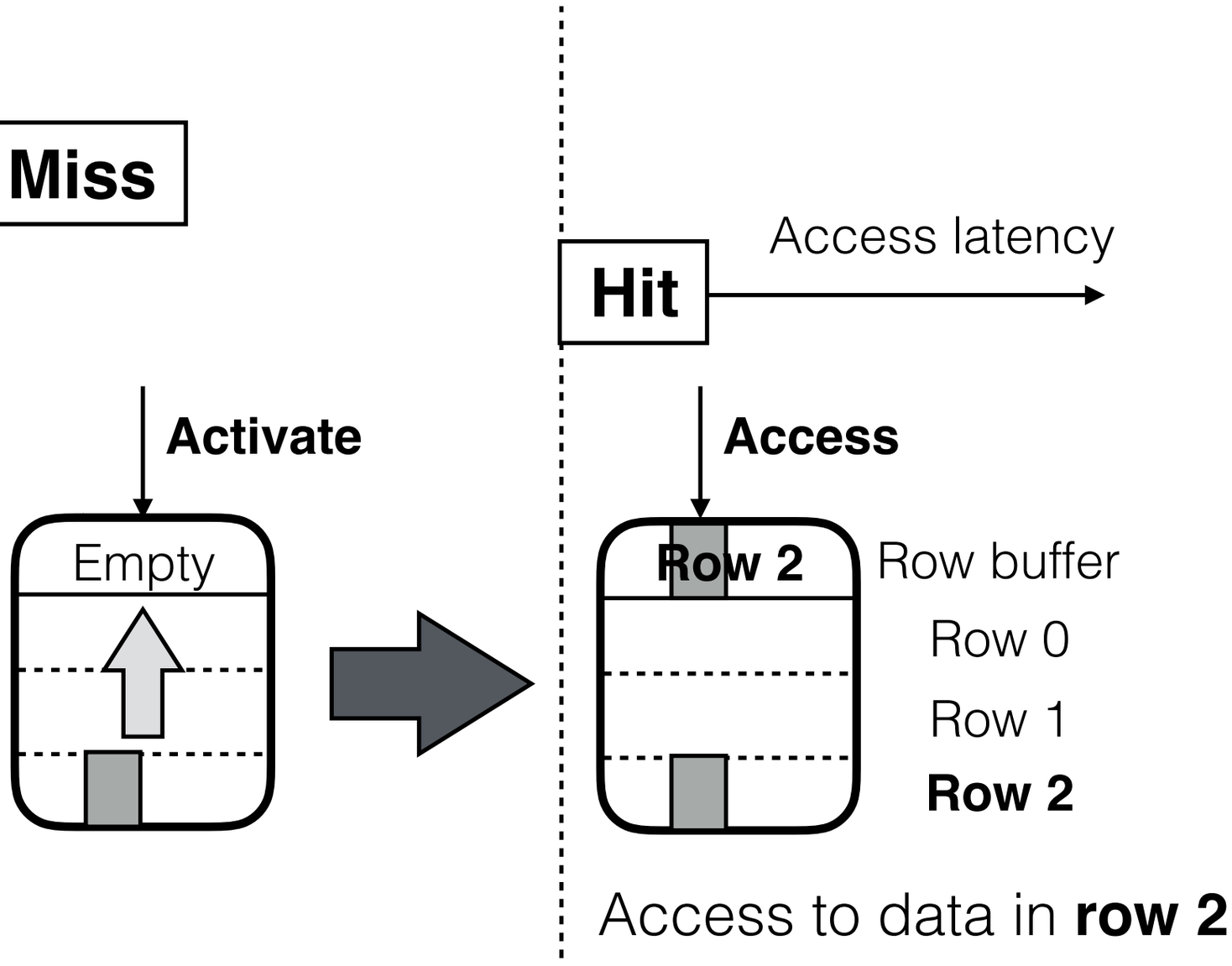

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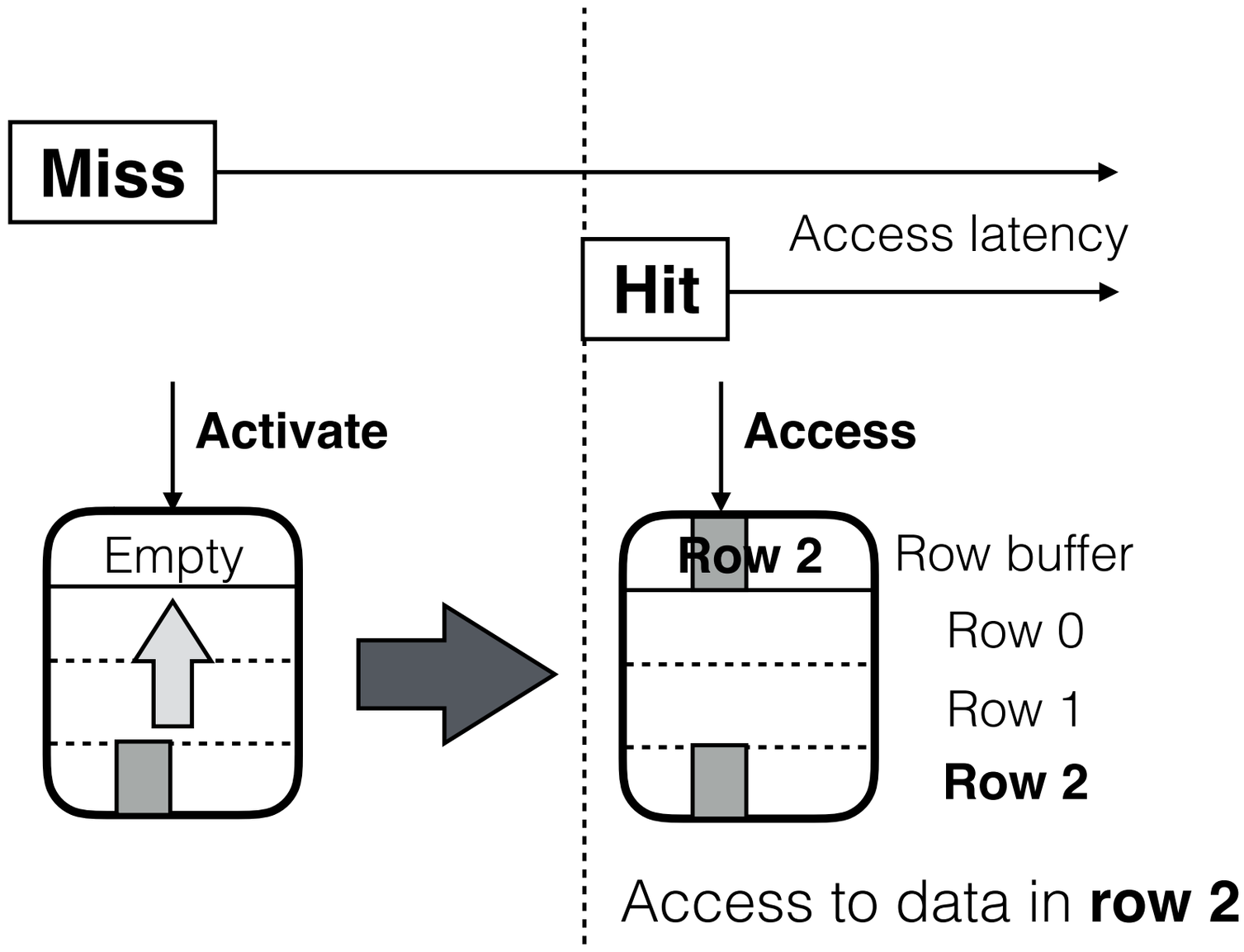

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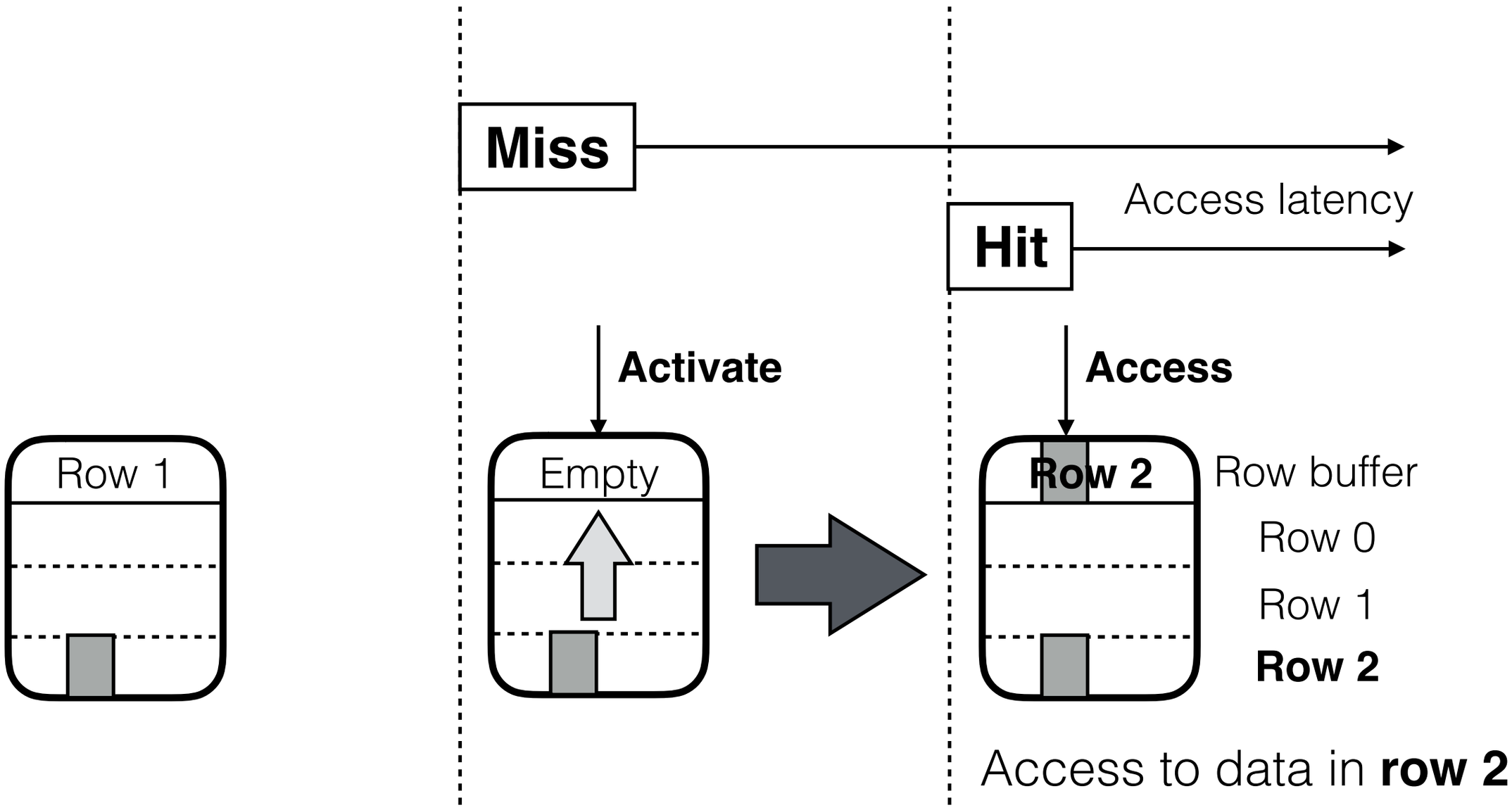

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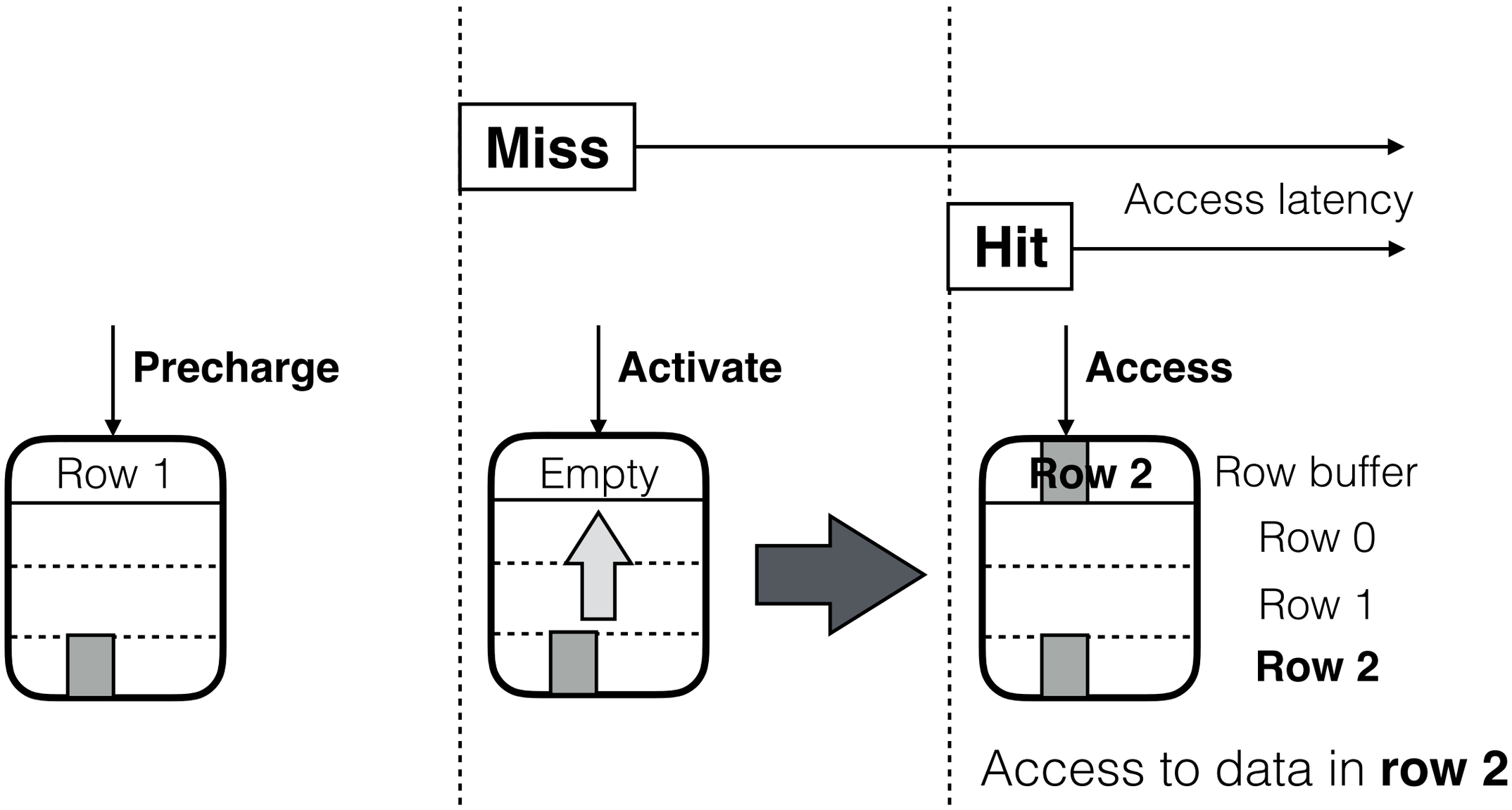

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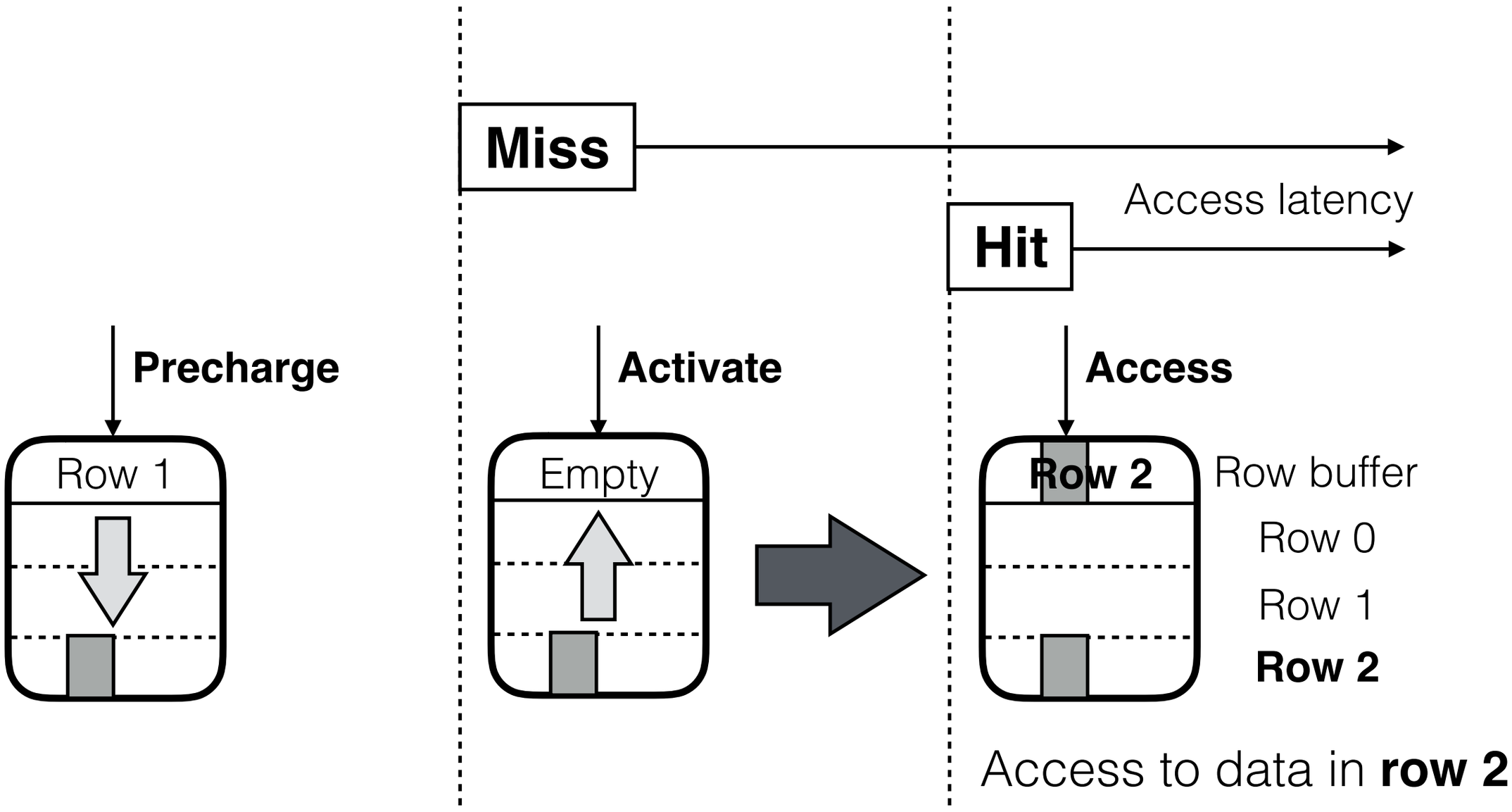

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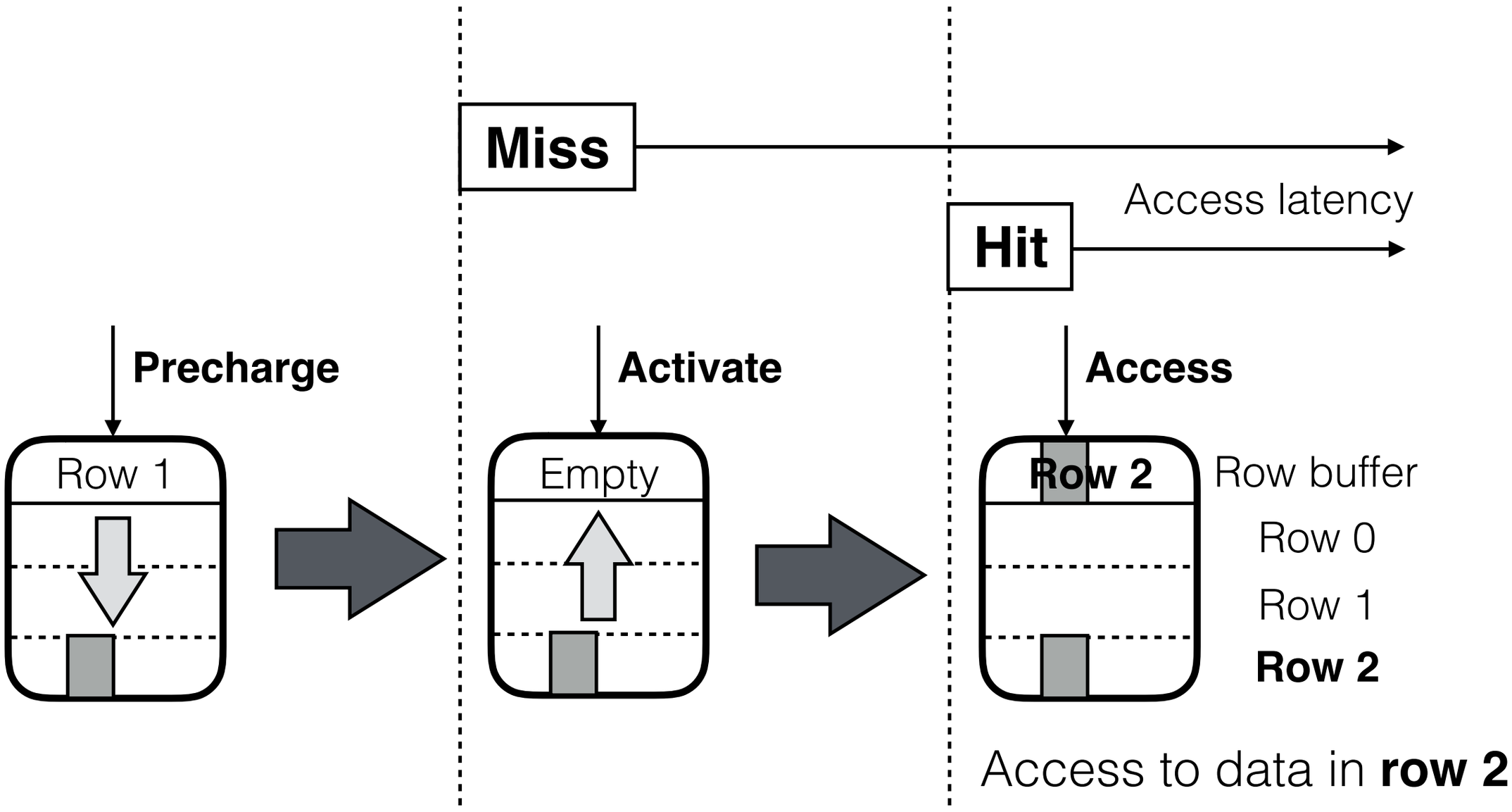

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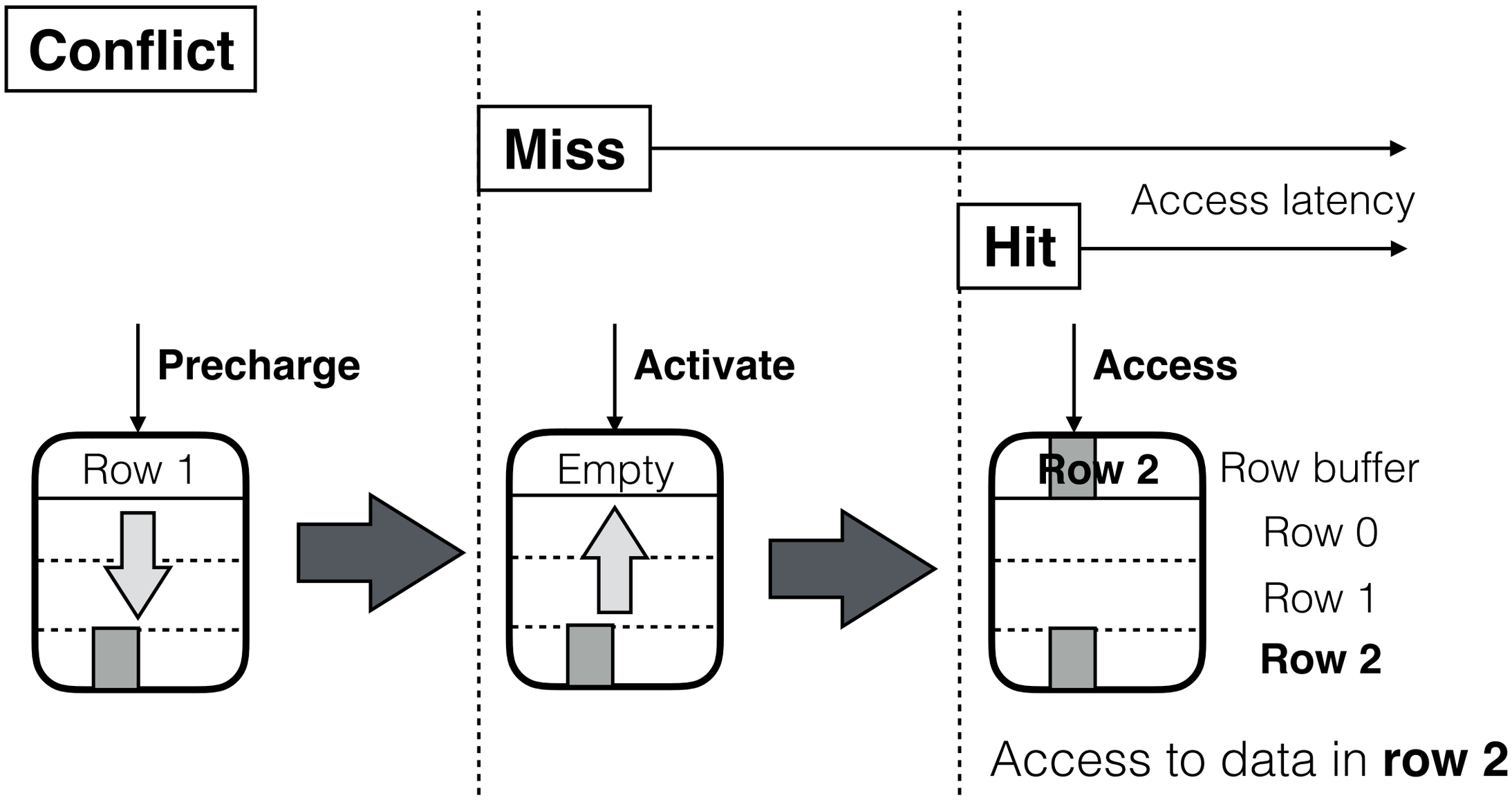

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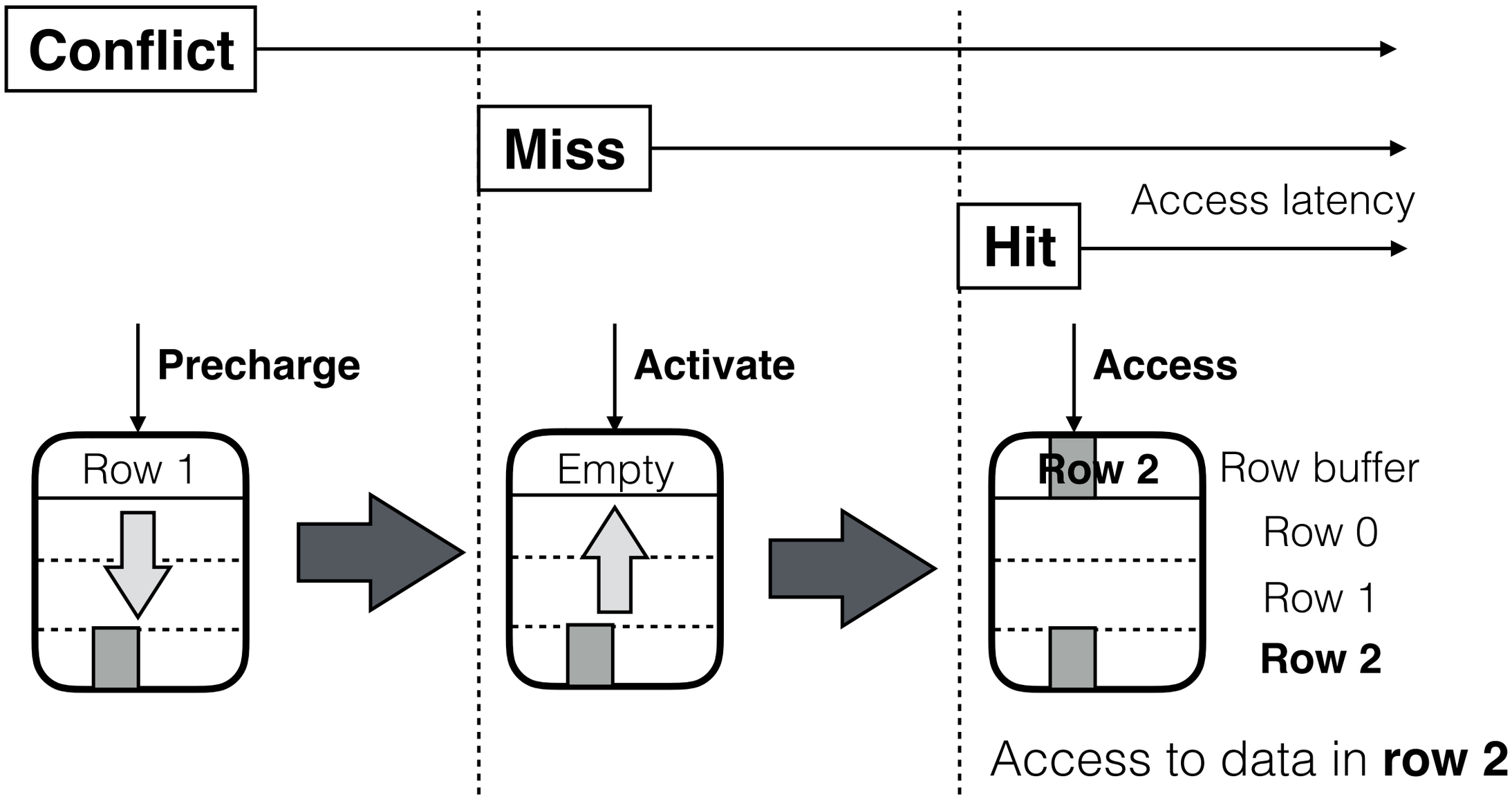

Row Buffer Management Polices

- Open-page policy
  - Row buffers are NOT precharged (closed) after accessed
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Used in this work

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Agenda

- State-of-the-art BFS implementation
- DRAM mechanisms
- Memory access analysis with conventional address mapping schemes
- Proposed: per-row channel interleaving
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Address Mapping Schemes

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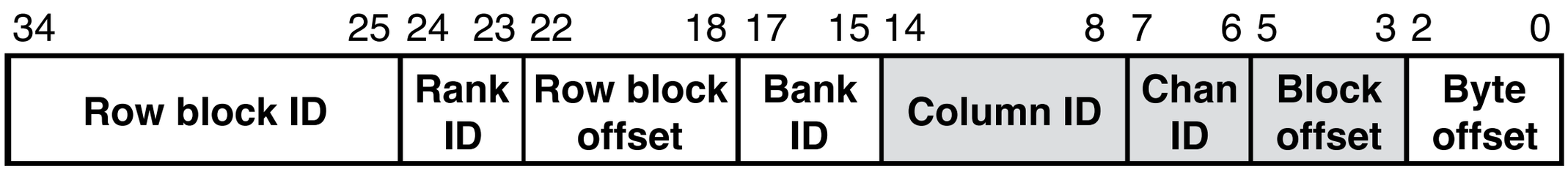
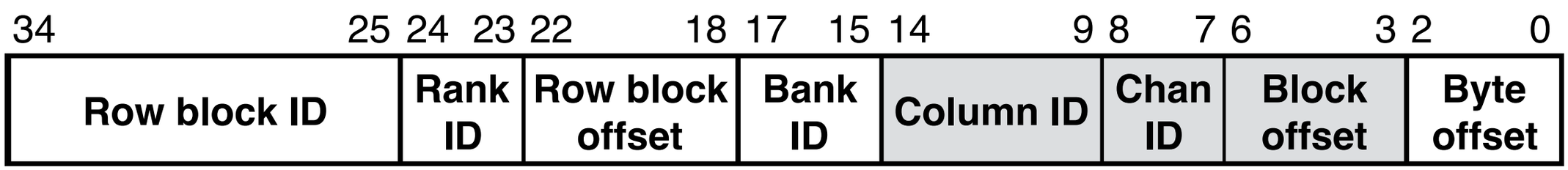
- Conventional schemes:
  - Per-cache-line channel interleaving (PCL)
    - ✓ 64 B blocks are interleaved across channels
    - ✓ Applied to Intel Nehalem processors [Park+, ASPLOS ’13]
  - Per-2-cache-line channel interleaving (P2CL)
    - ✓ 128 B blocks are interleaved across channels
    - ✓ Applied to Intel SandyBridge and Haswell processors

Breakdown of Physical Addresses

Per-cache-line channel interleaving (PCL)



Per-2-cache-lines channel interleaving (P2CL)



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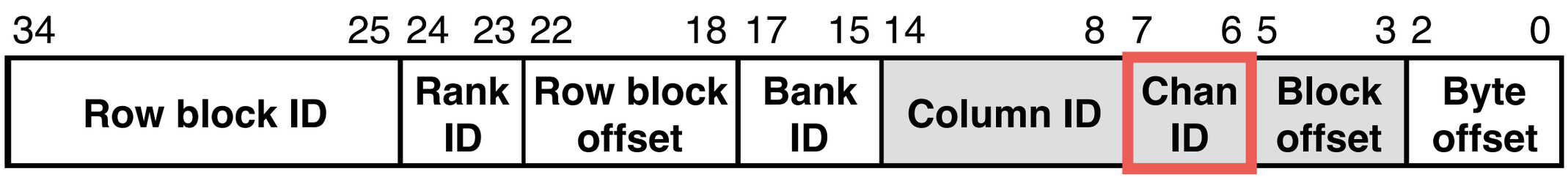
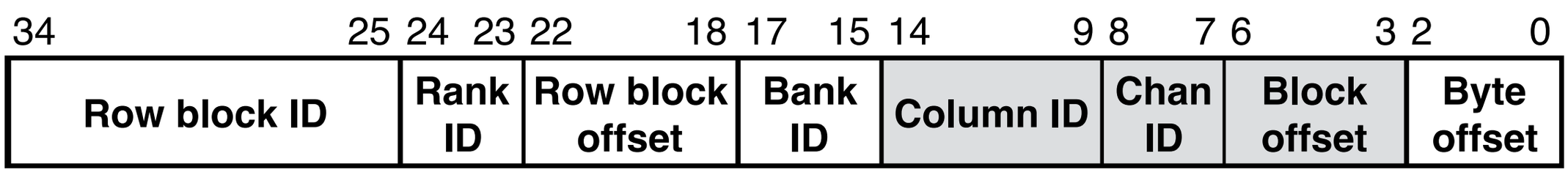
Per-cache-line channel interleaving (PCL)



Per-2-cache-lines channel interleaving (P2CL)



Breakdown of Physical Addresses

Per-cache-line channel interleaving (PCL)

6 bits → 64 B

34	25	24	23	22	18	17	15	14	8	7	6	5	3	2	0
Row block ID		Rank ID		Row block offset		Bank ID		Column ID		Chan ID		Block offset		Byte offset	

Per-2-cache-lines channel interleaving (P2CL)

34	25	24	23	22	18	17	15	14	9	8	7	6	3	2	0
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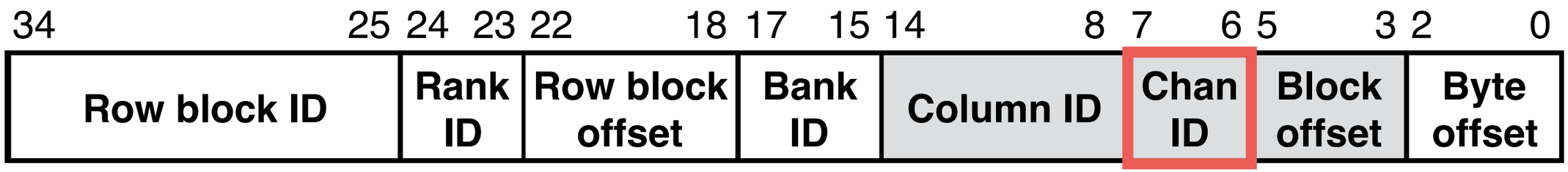
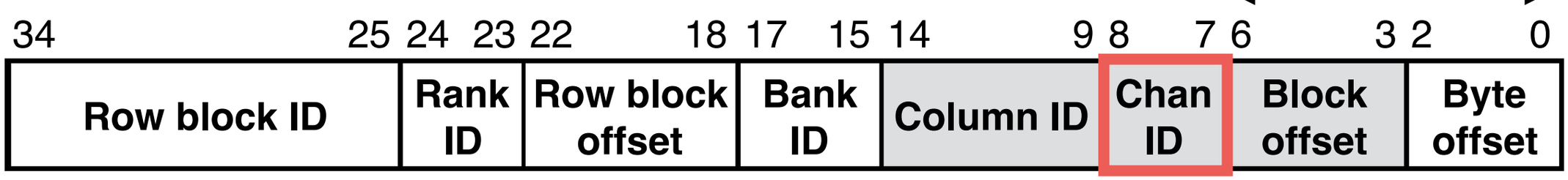


Per-2-cache-lines channel interleaving (P2CL)

7 bits → 128 B



Simulator Setup

- Cycle-accurate multicore simulator: MARSSx86
- DRAM simulator: DRAMsim2

Simulator Setup

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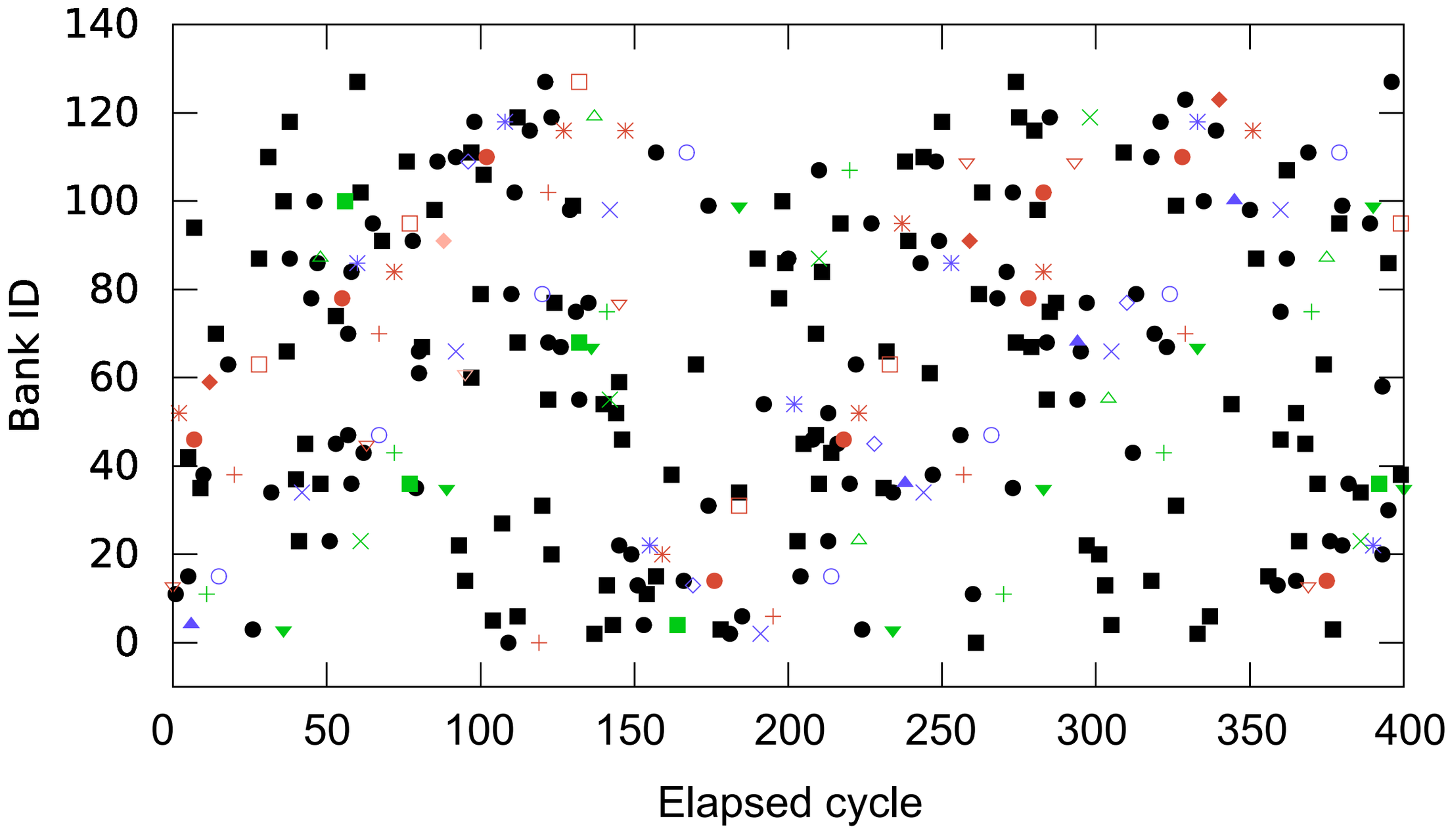
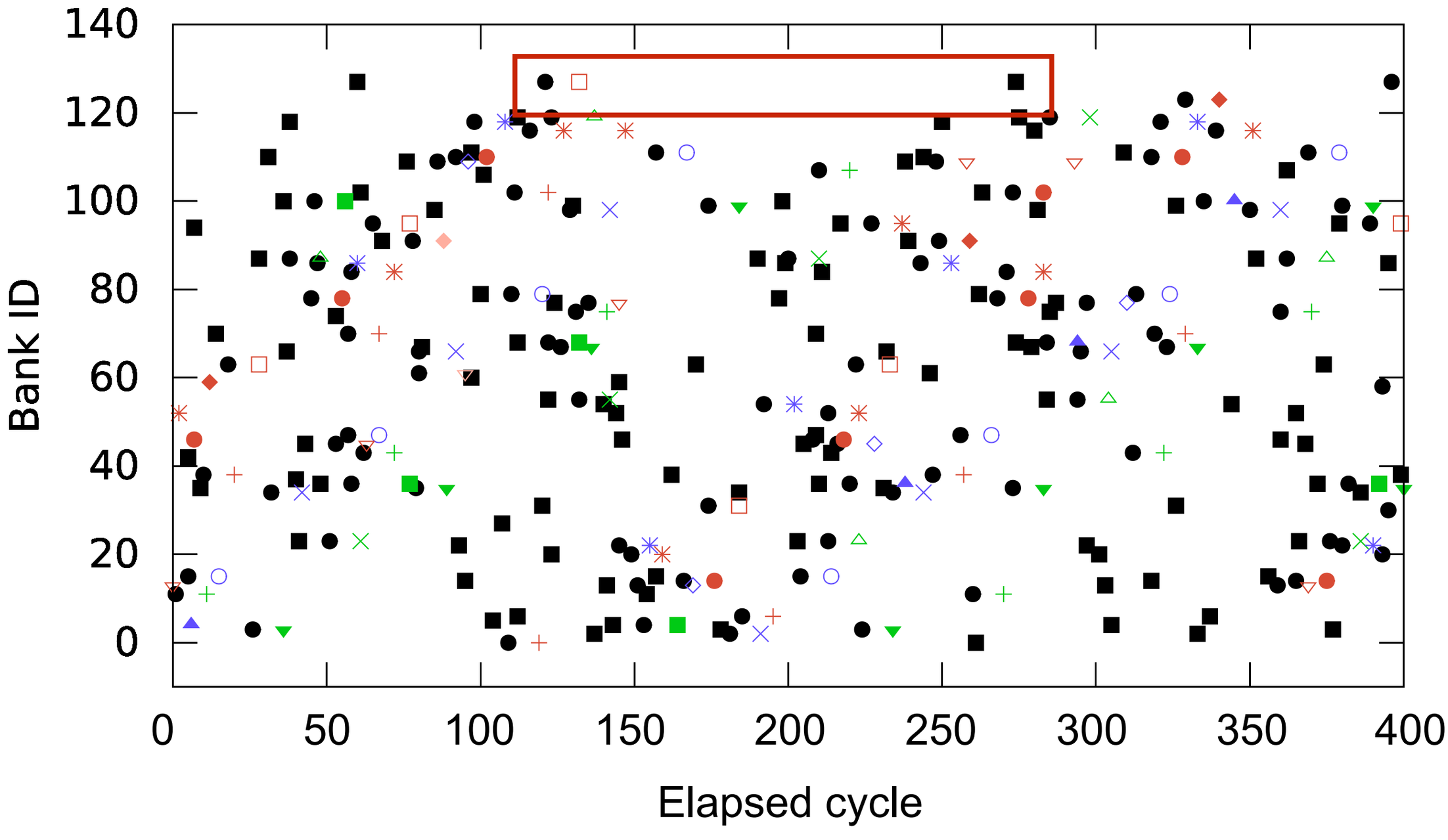
- DRAM simulator: DRAMsim2

Parameter	Setting
Processor	**16 Out-of-Order cores**, 3.0 GHz
Cache	Private 32 KB L1 I/D, Private 256 KB L2 Shared 16 MB L3
Memory Controller	**Adaptive open-page policy (128 cycles)** FR-FCFS scheduling policy [Rixner+, ISCA'00]
DRAM	**32 GB, DDR3-1333, 8 KB row** **4 channels, 4 ranks/channel, 8 banks/rank (128 banks)**

Memory Access Trace of Bottom-up with PCL



Memory Access Trace of Bottom-up with PCL



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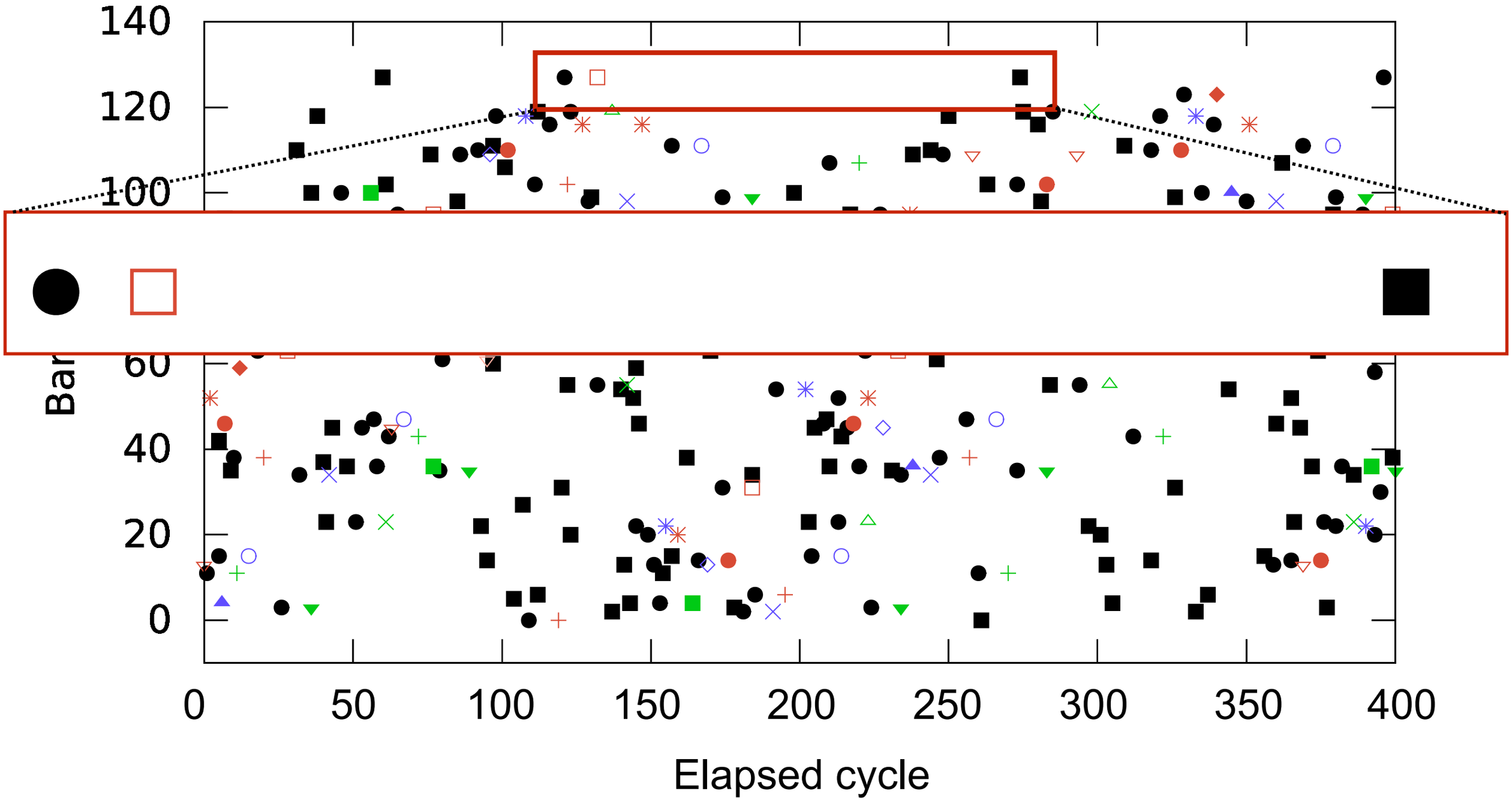

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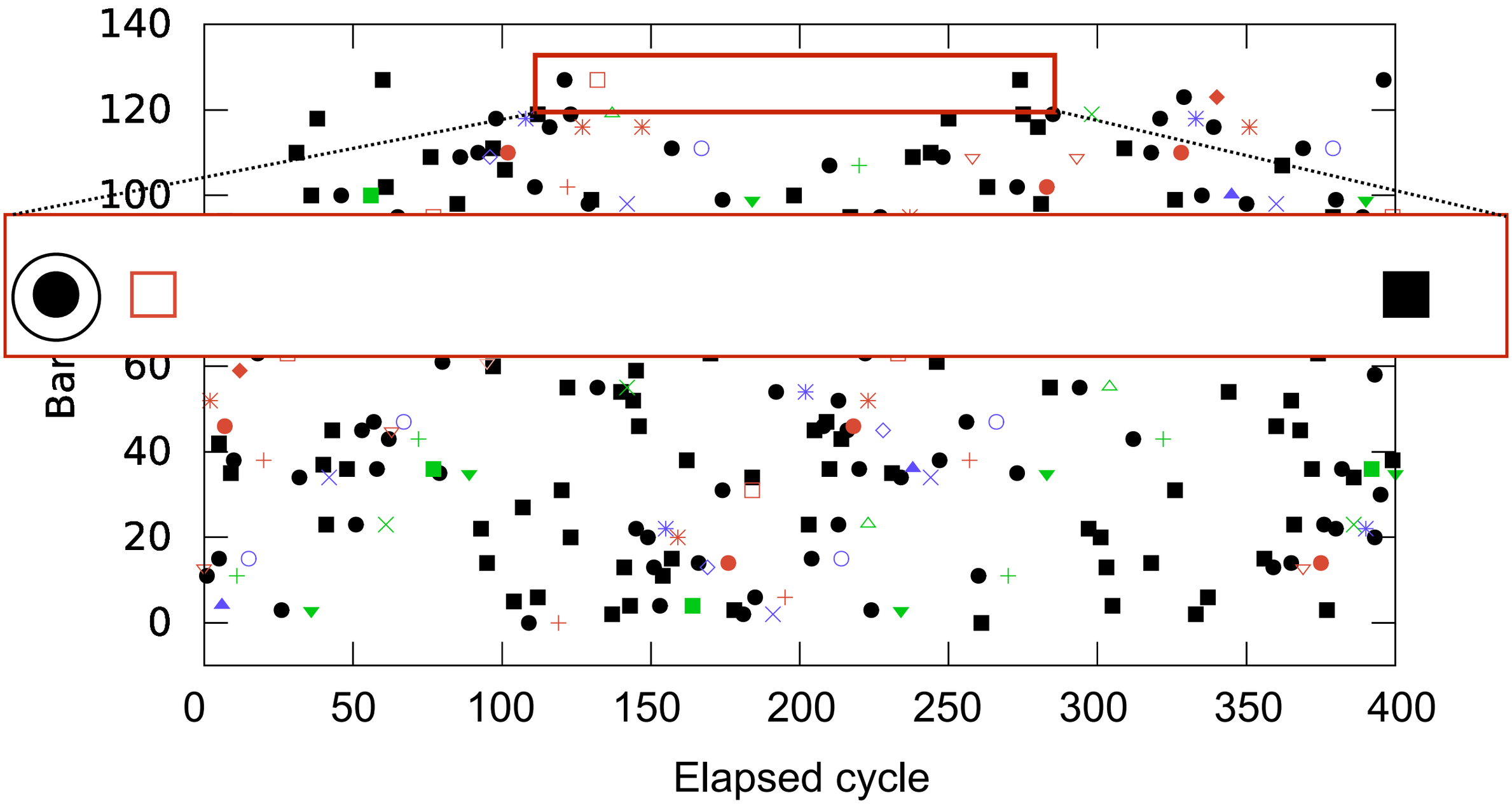
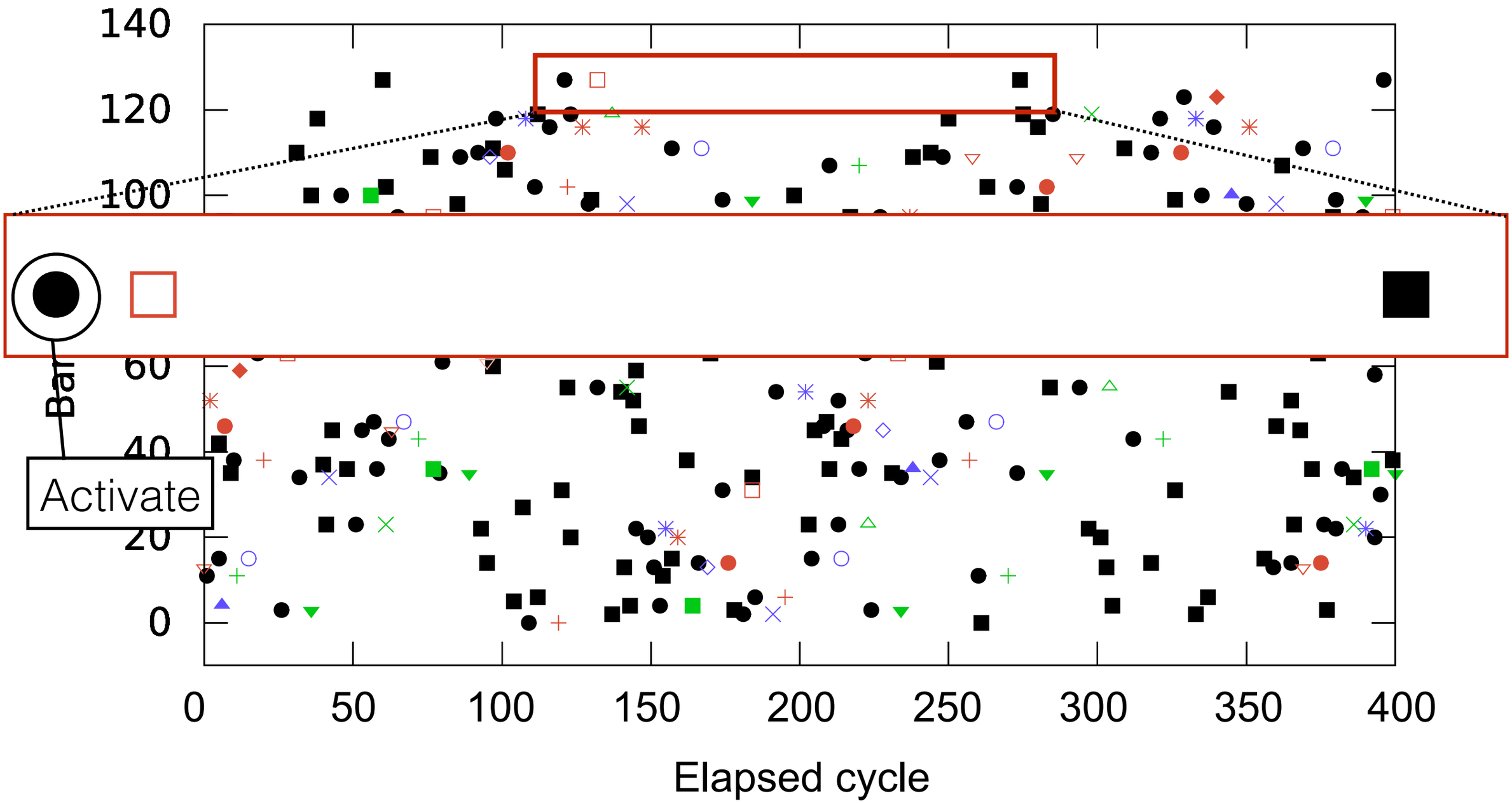


Memory Access Trace of Bottom-up with PCL



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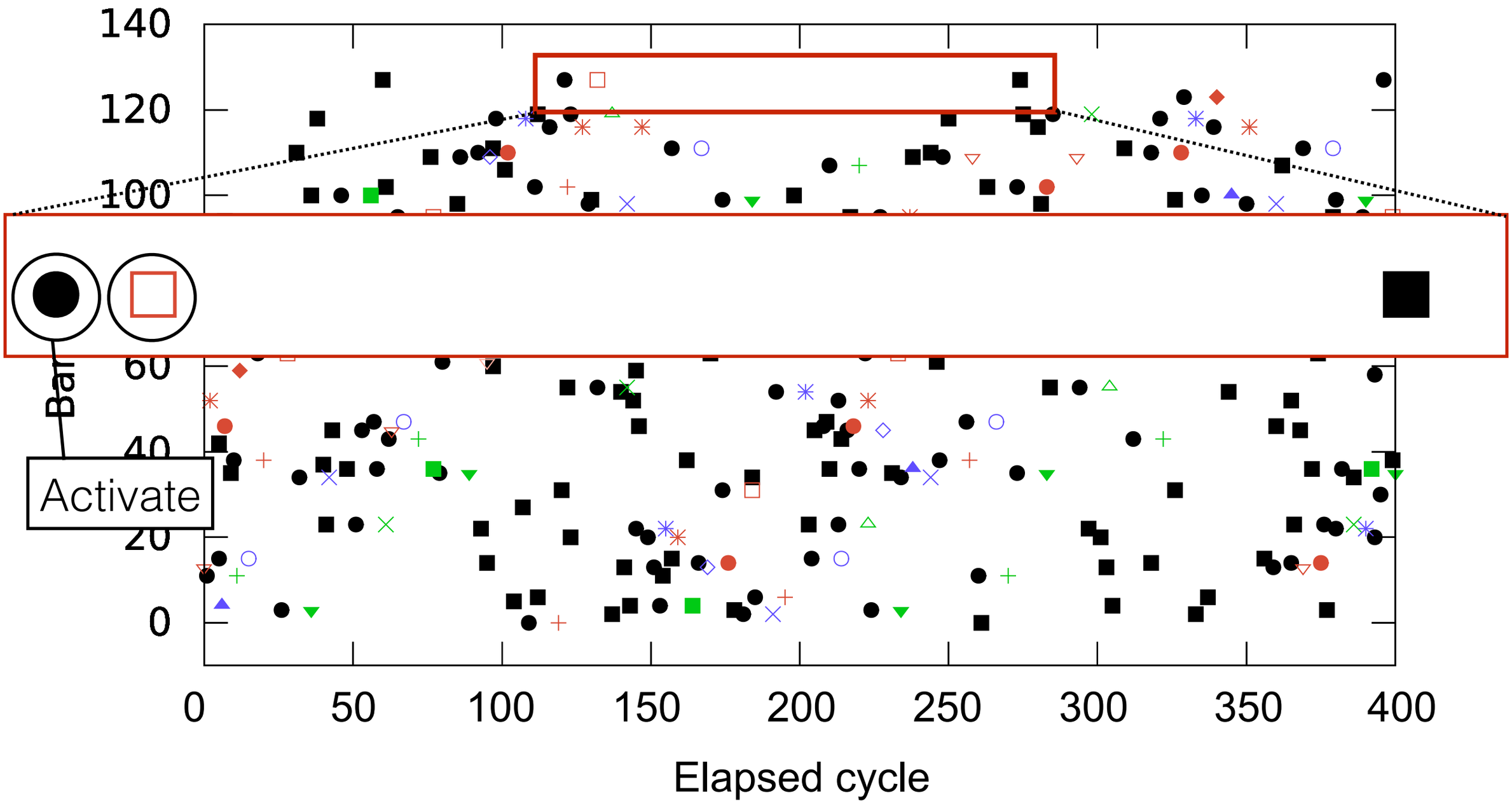

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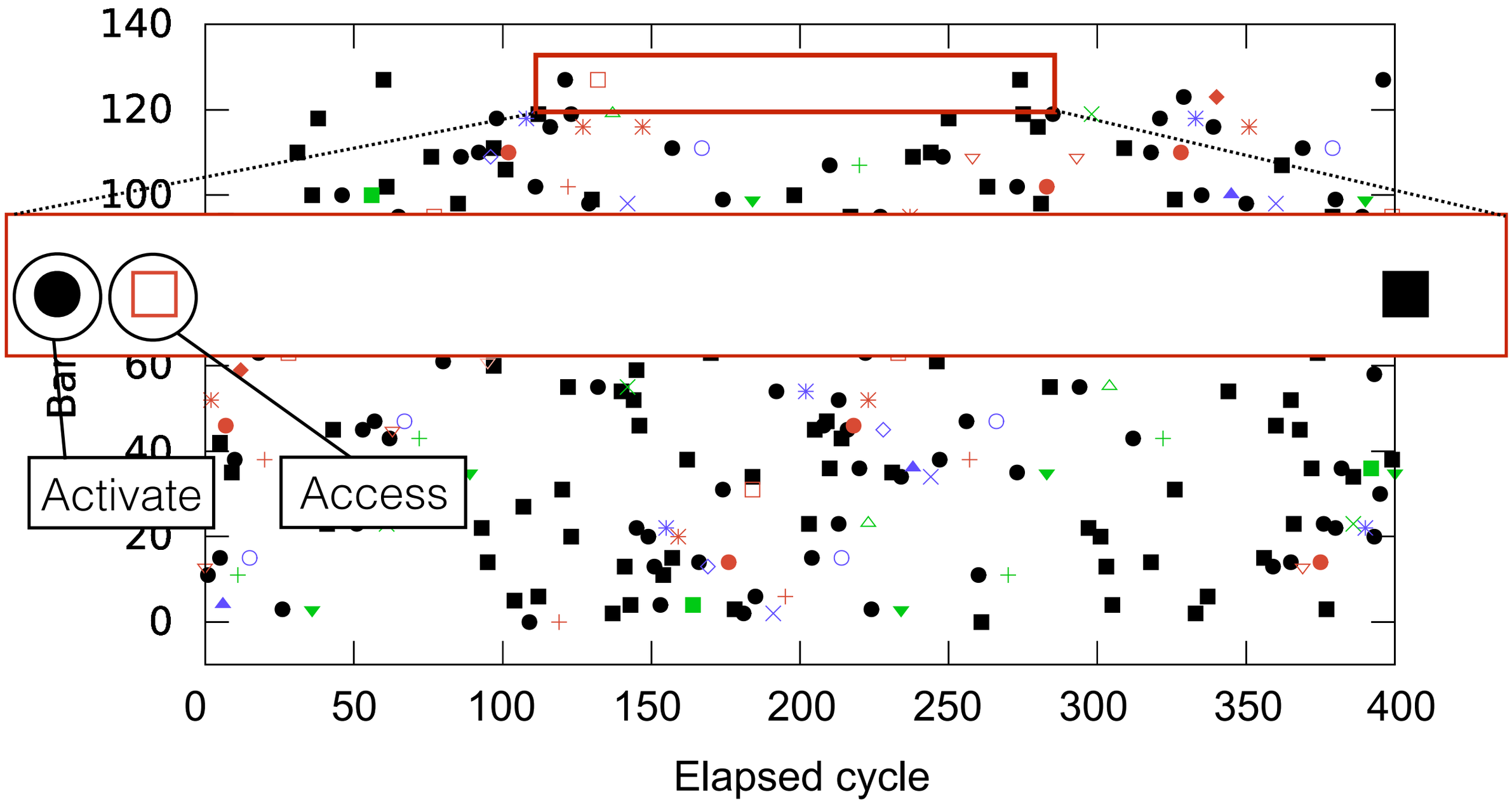

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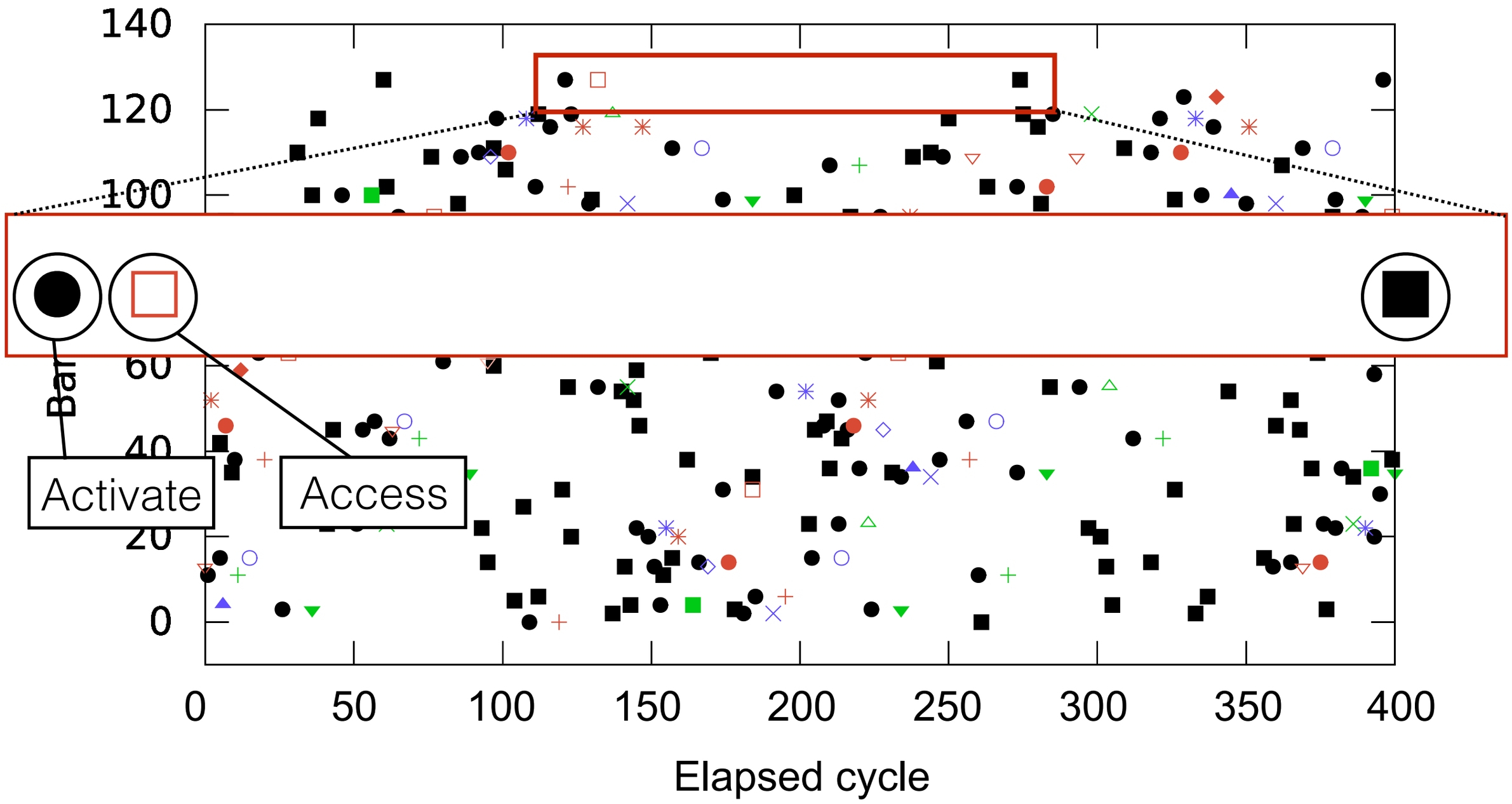

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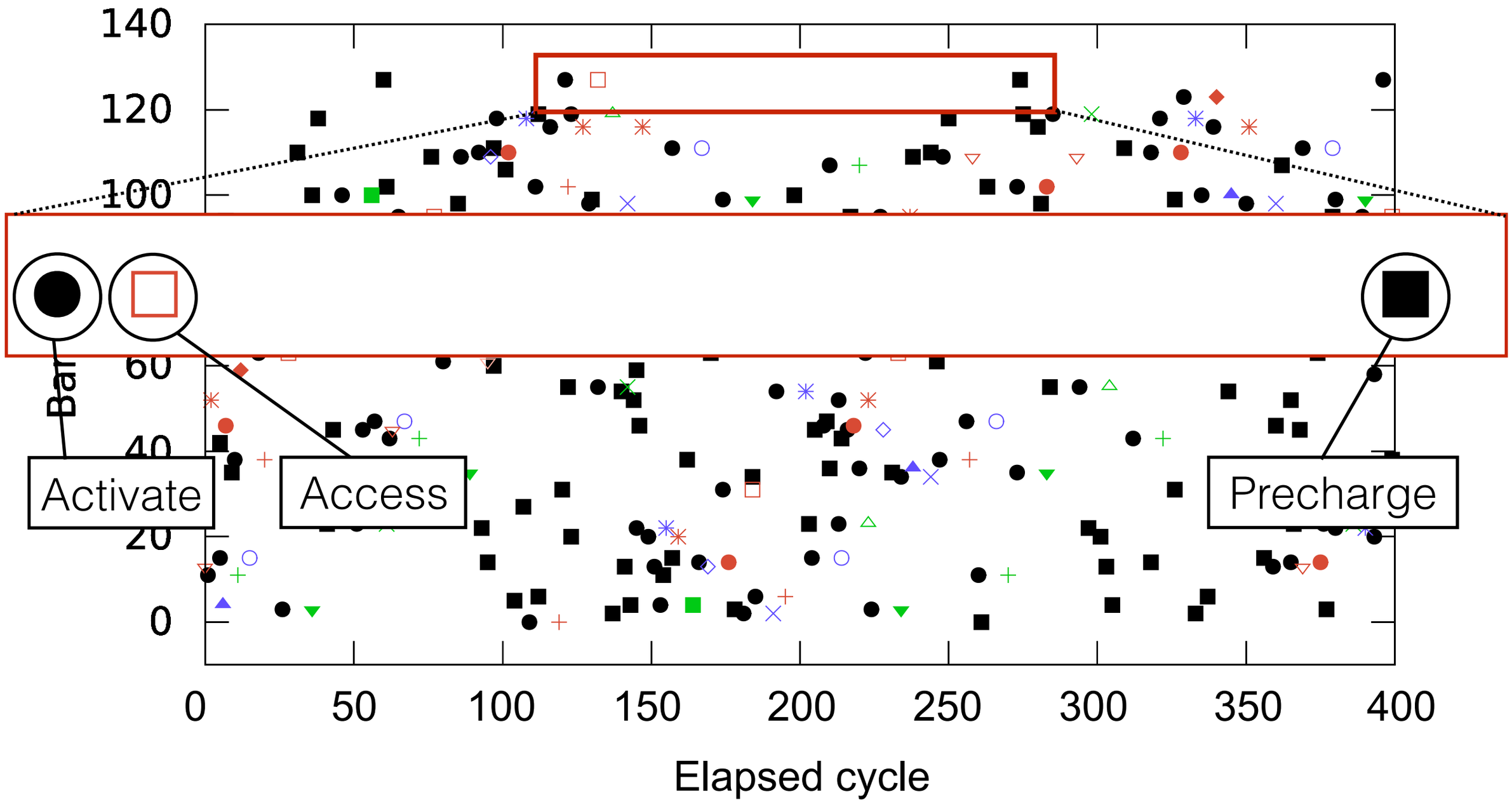

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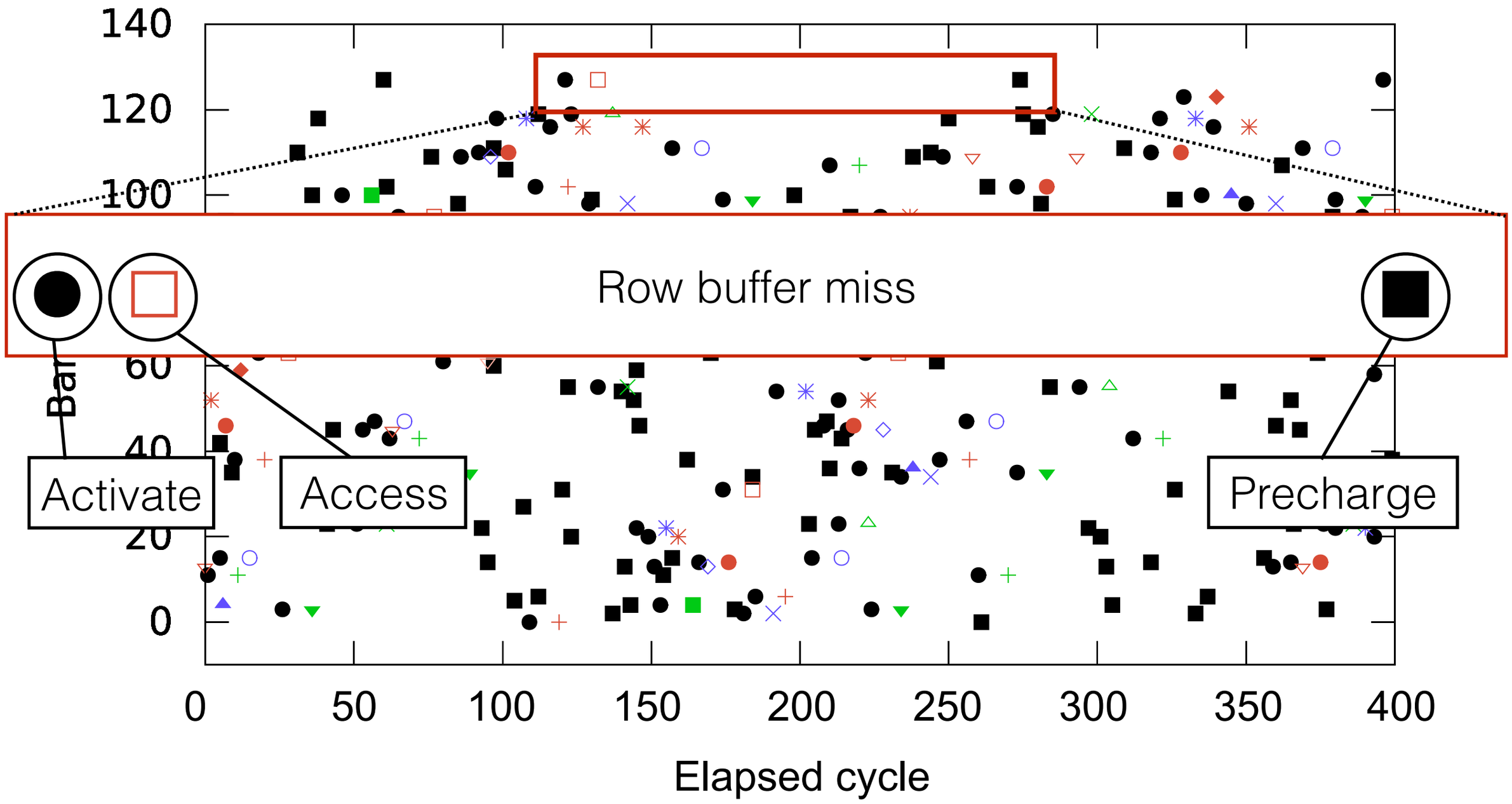

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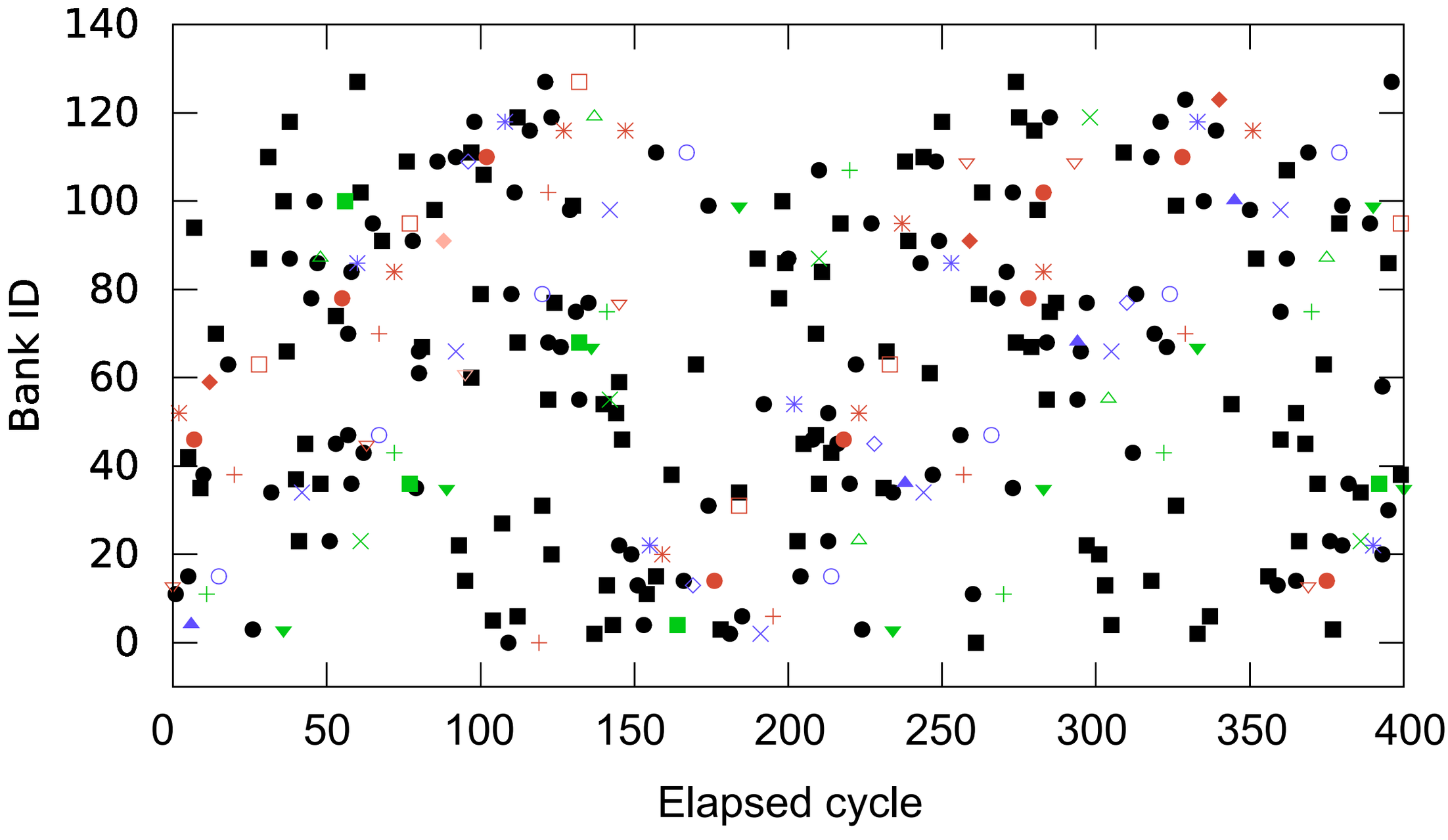

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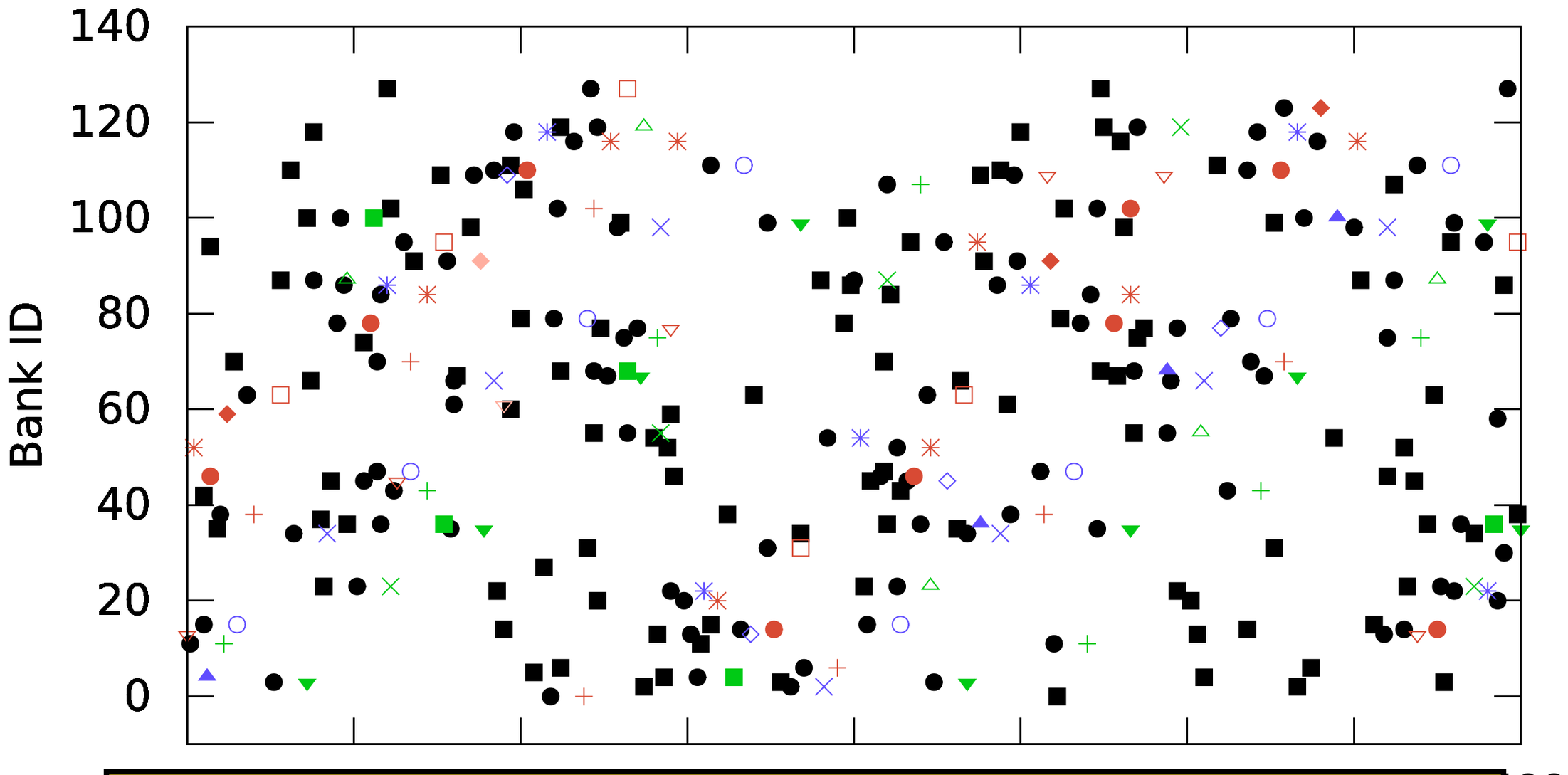
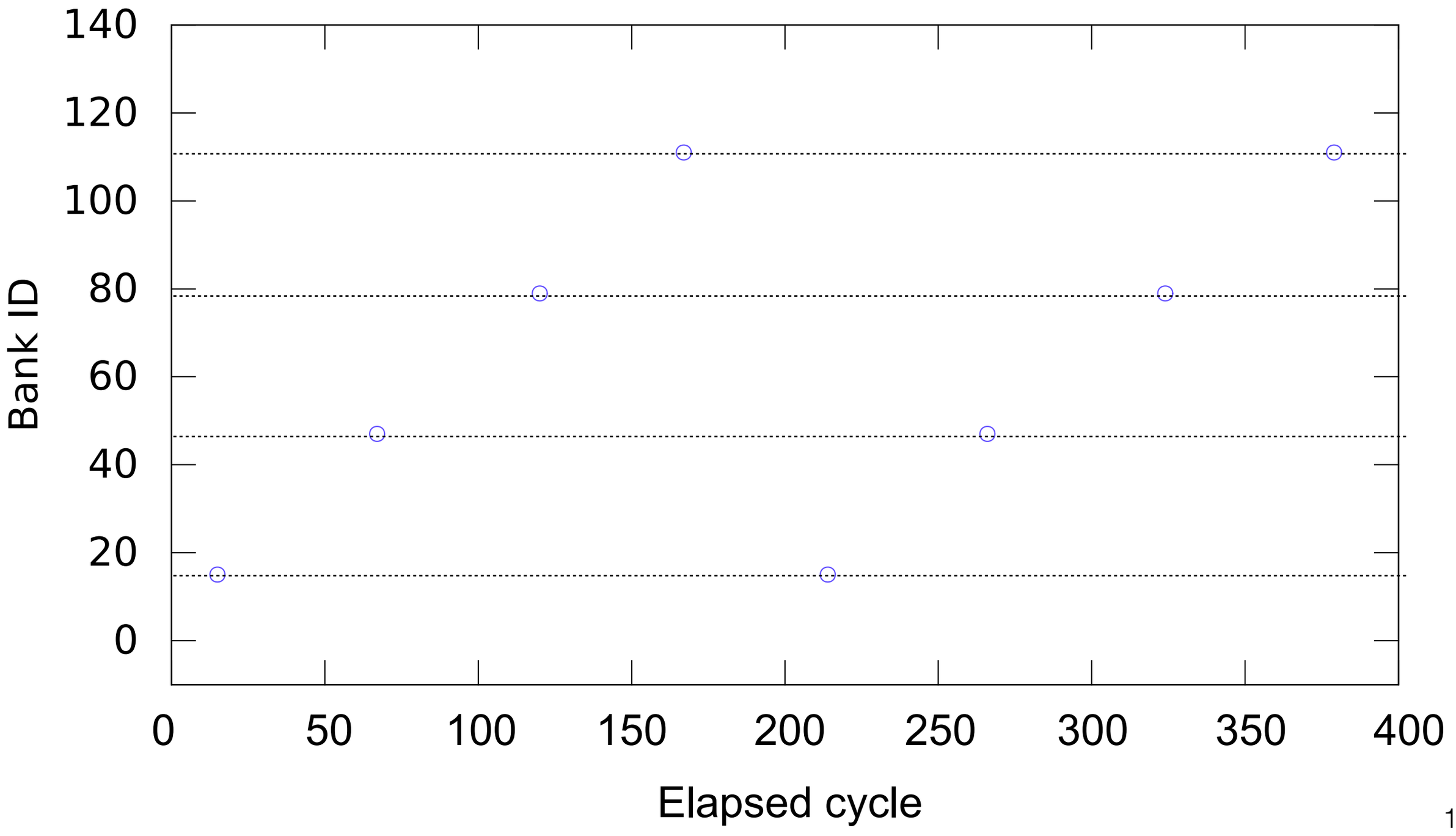


- Almost all accesses are row buffer misses
- Almost all threads access distinct banks

Memory Access Trace of Bottom-up with PCL (1 thread)



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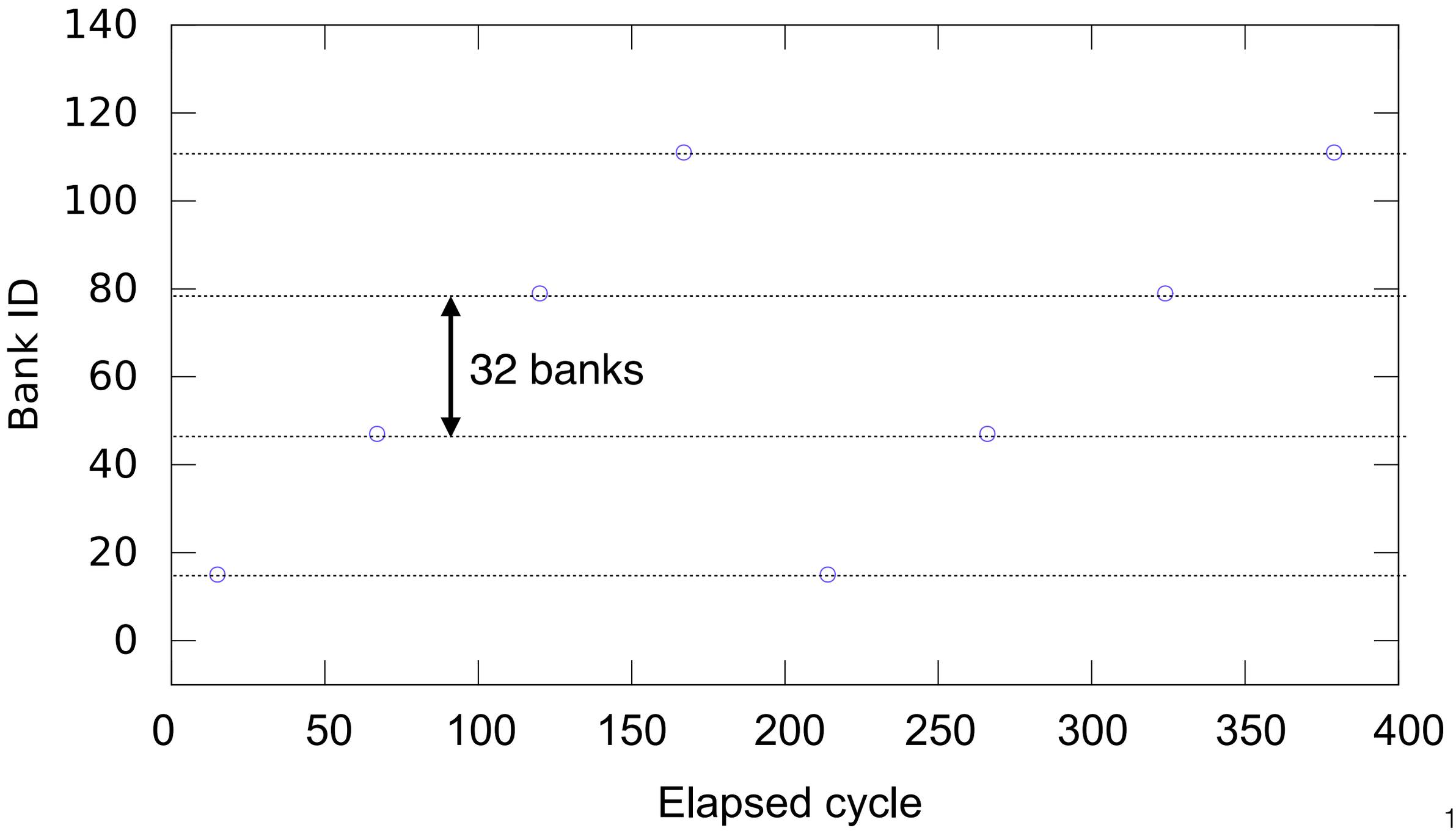

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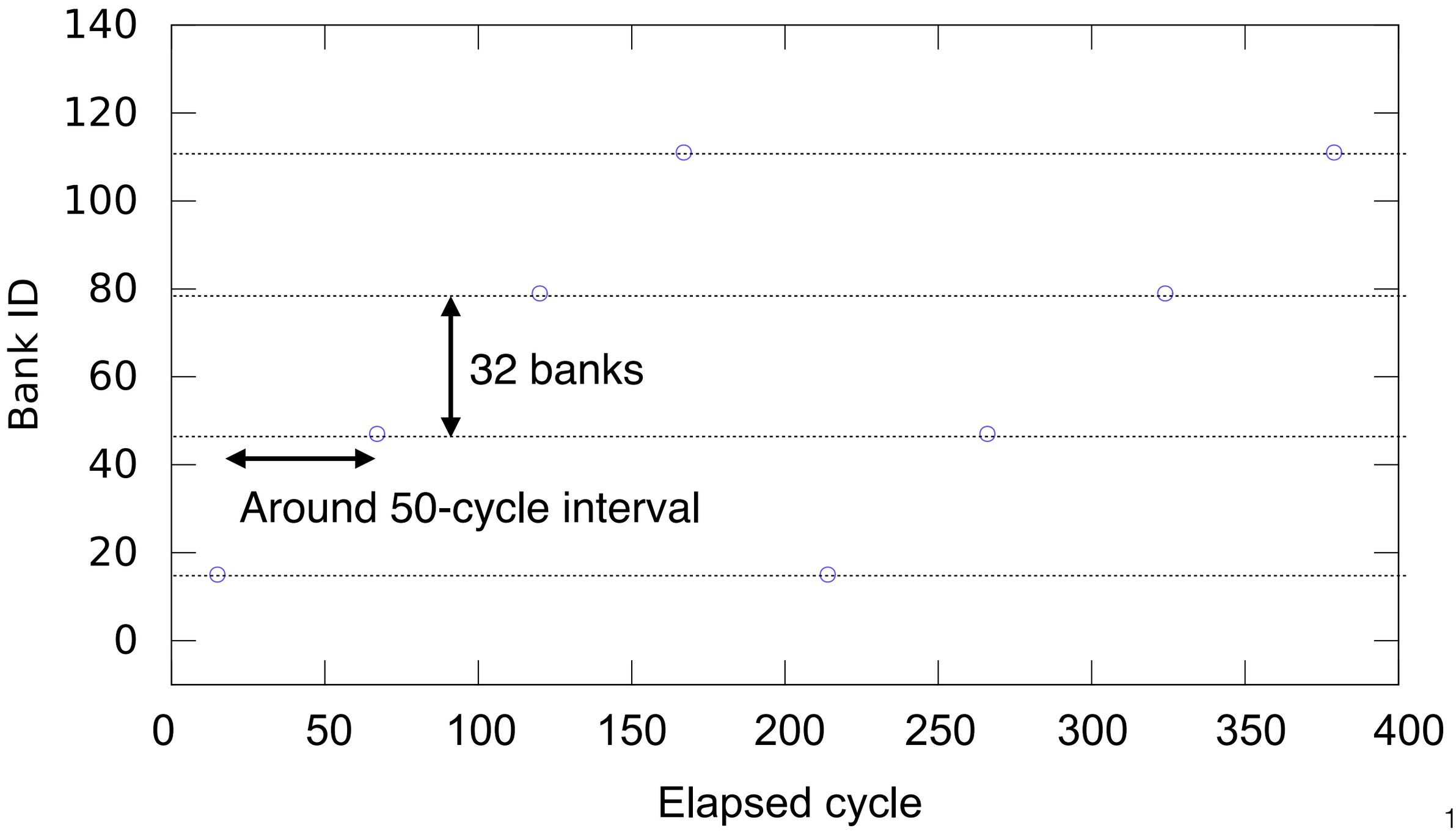

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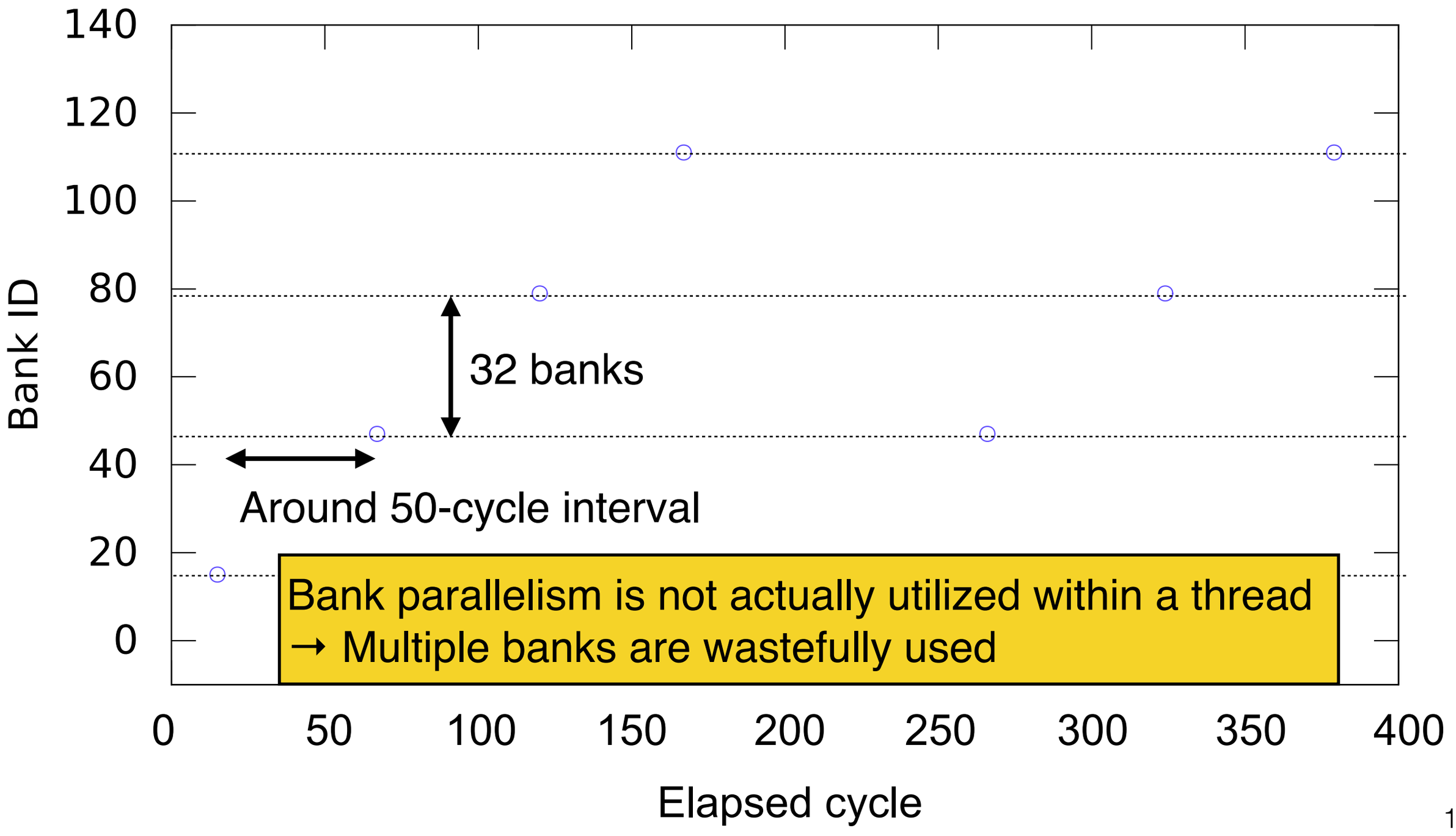

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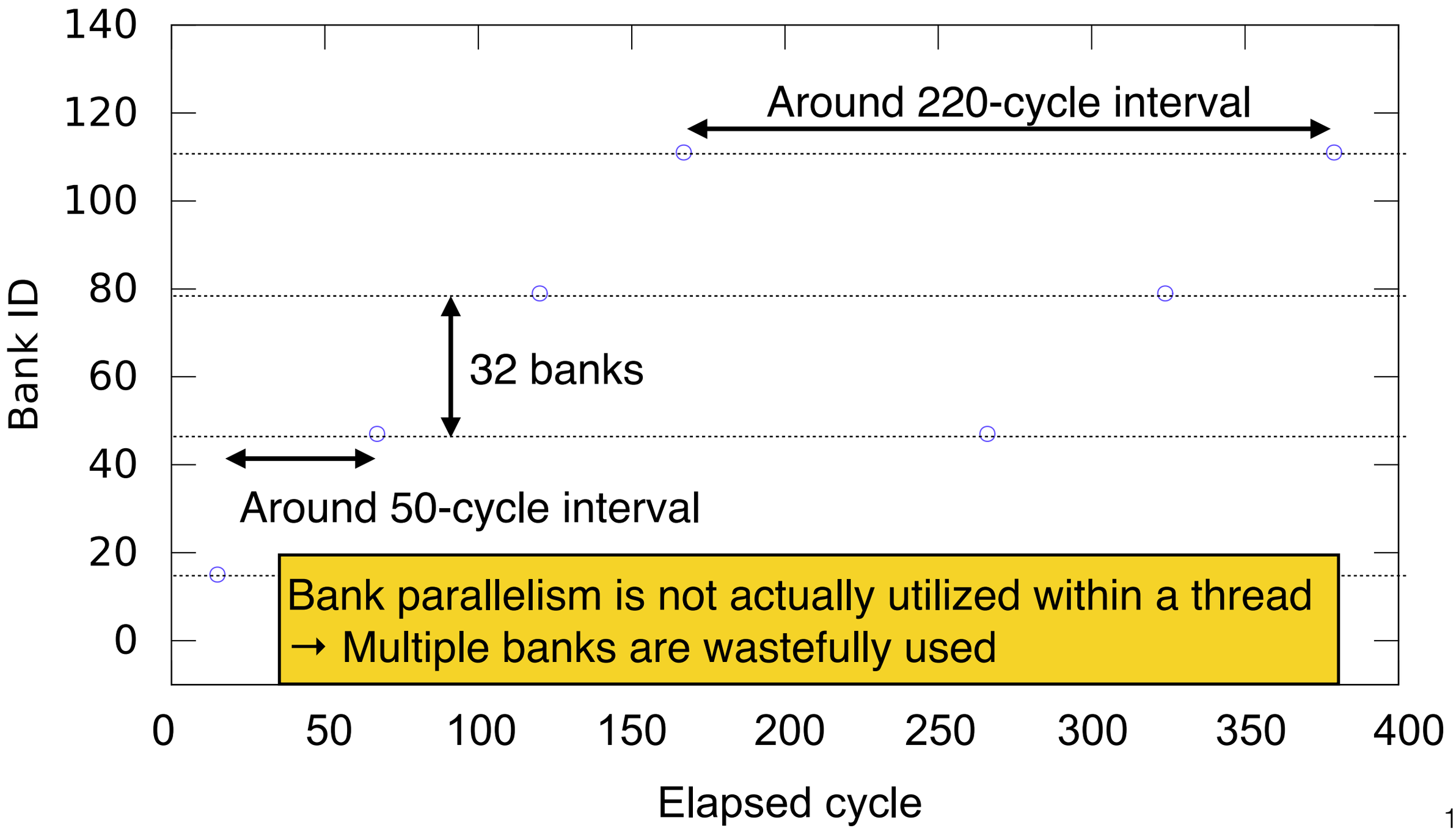

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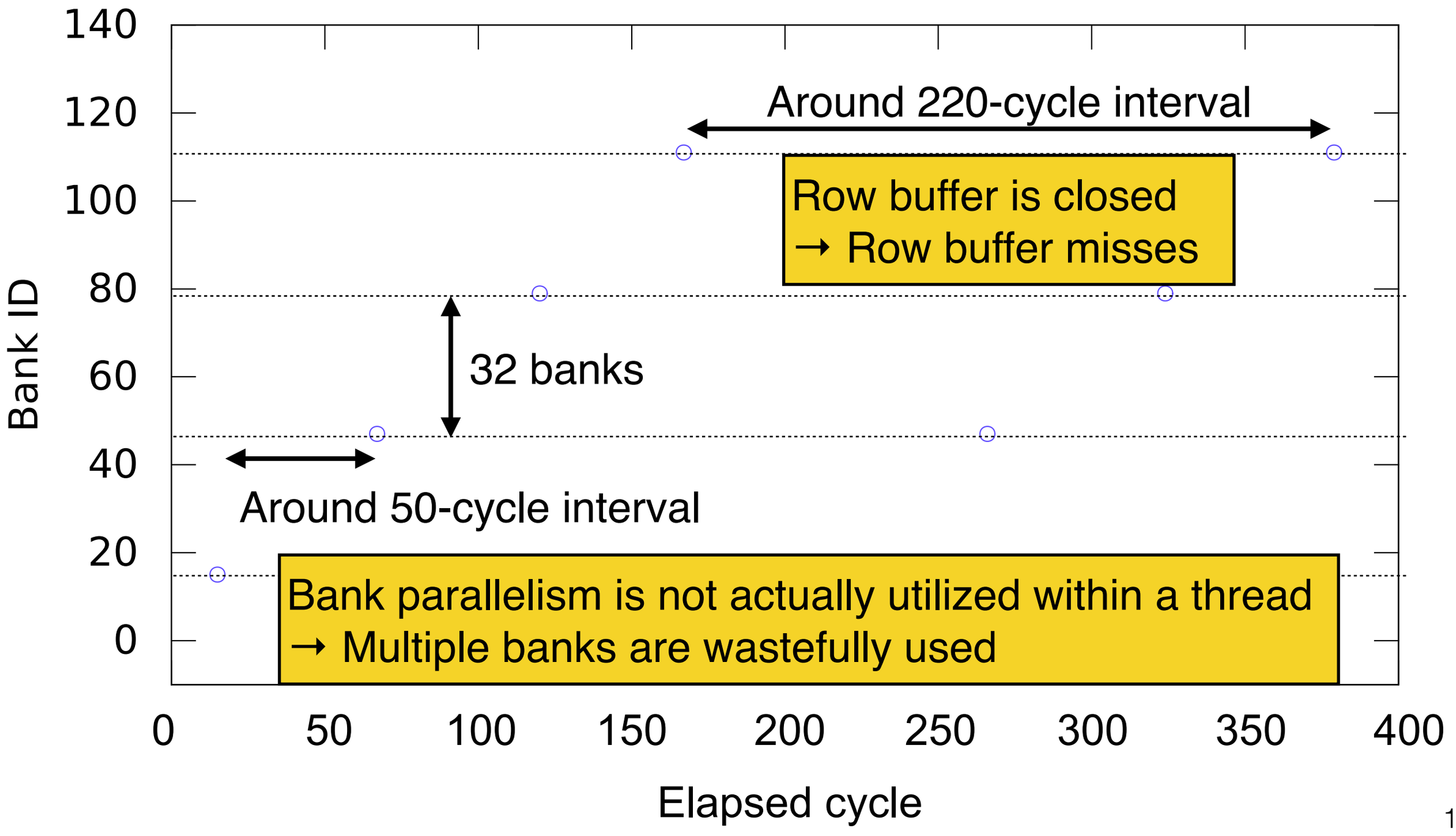

Agenda

- State-of-the-art BFS implementation
- DRAM mechanisms
- Memory access analysis with conventional address mapping schemes
- Proposed: per-row channel interleaving
- Evaluation of power efficiency

Idea

- If each thread sequentially accesses the entire row in the same bank…
  - Row buffer hit ratio (RBHR) should be improved
  - Bank parallelism should be exploited among different threads
  - #banks used at a time should be reduced

Per-Row Channel Interleaving (PR)

- Interleaves a contiguous memory region across channels per row size (8 KB in this work)

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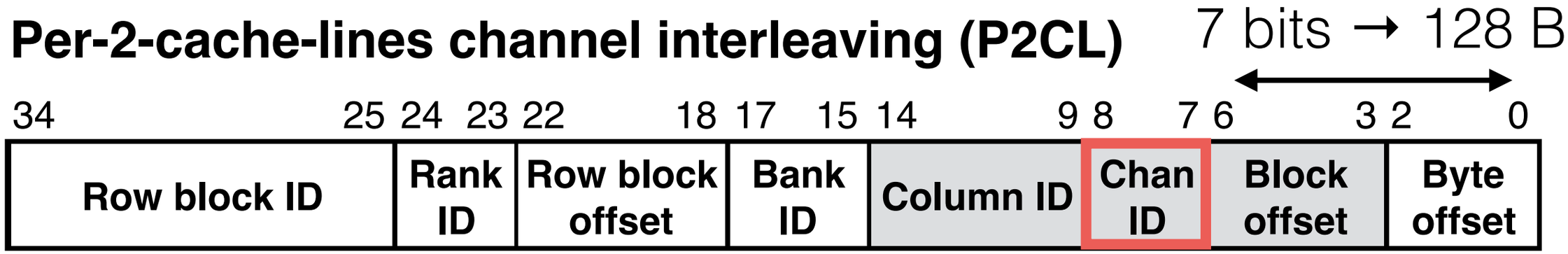

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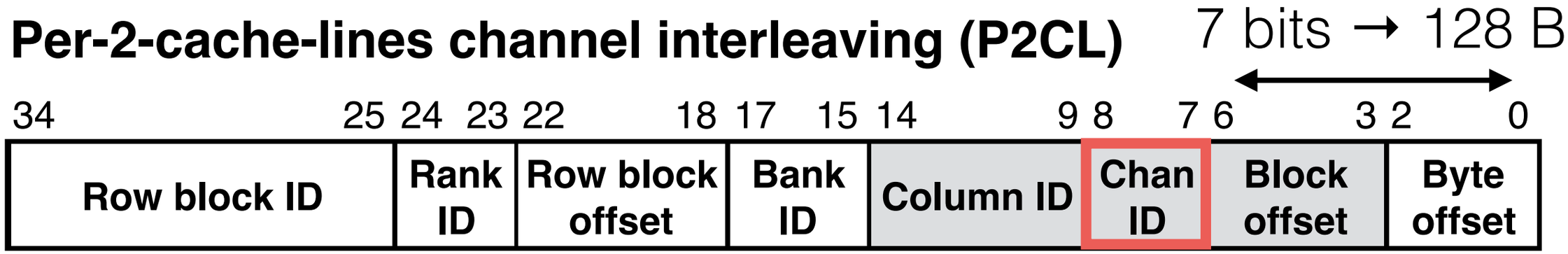

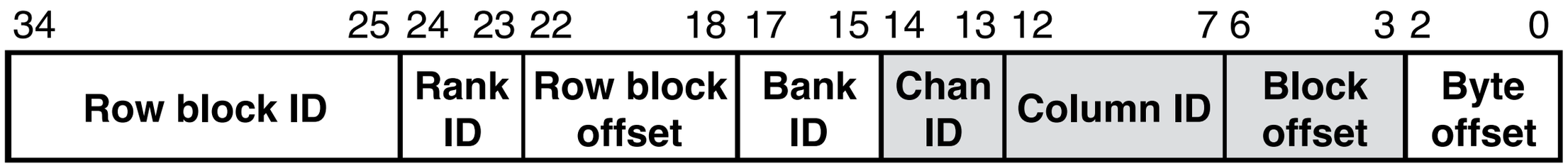

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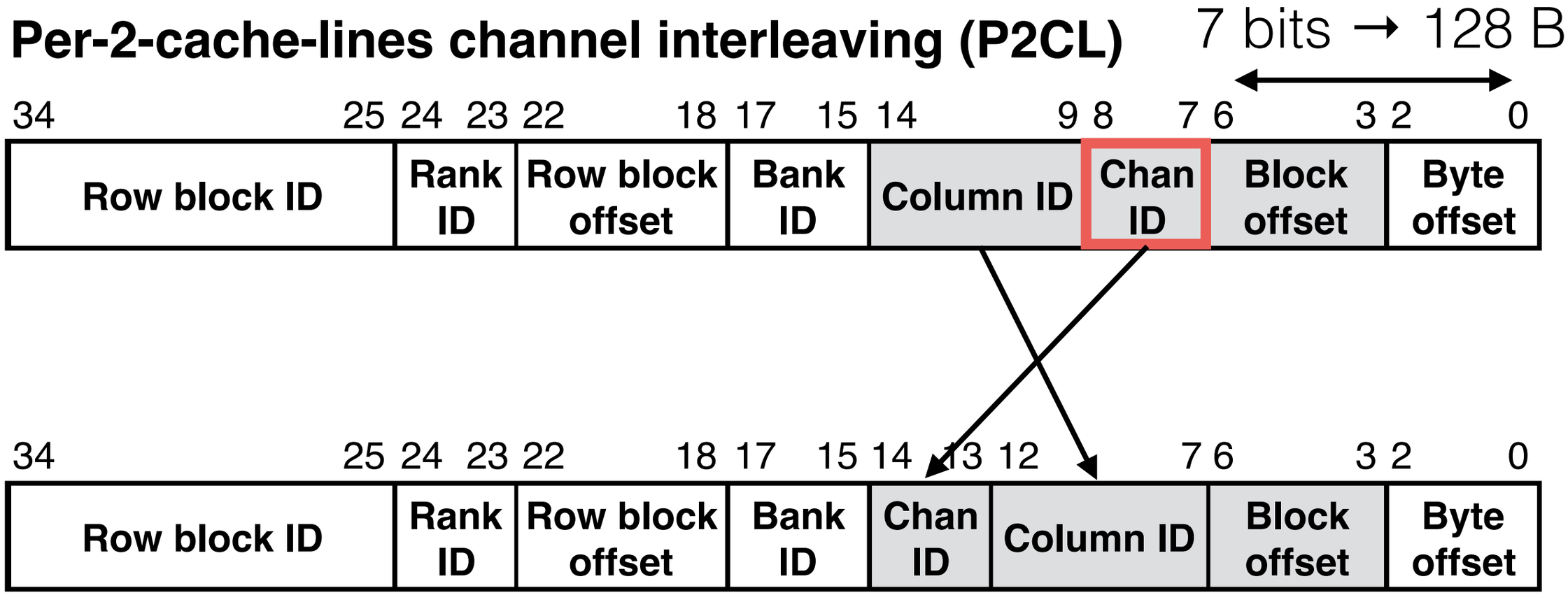

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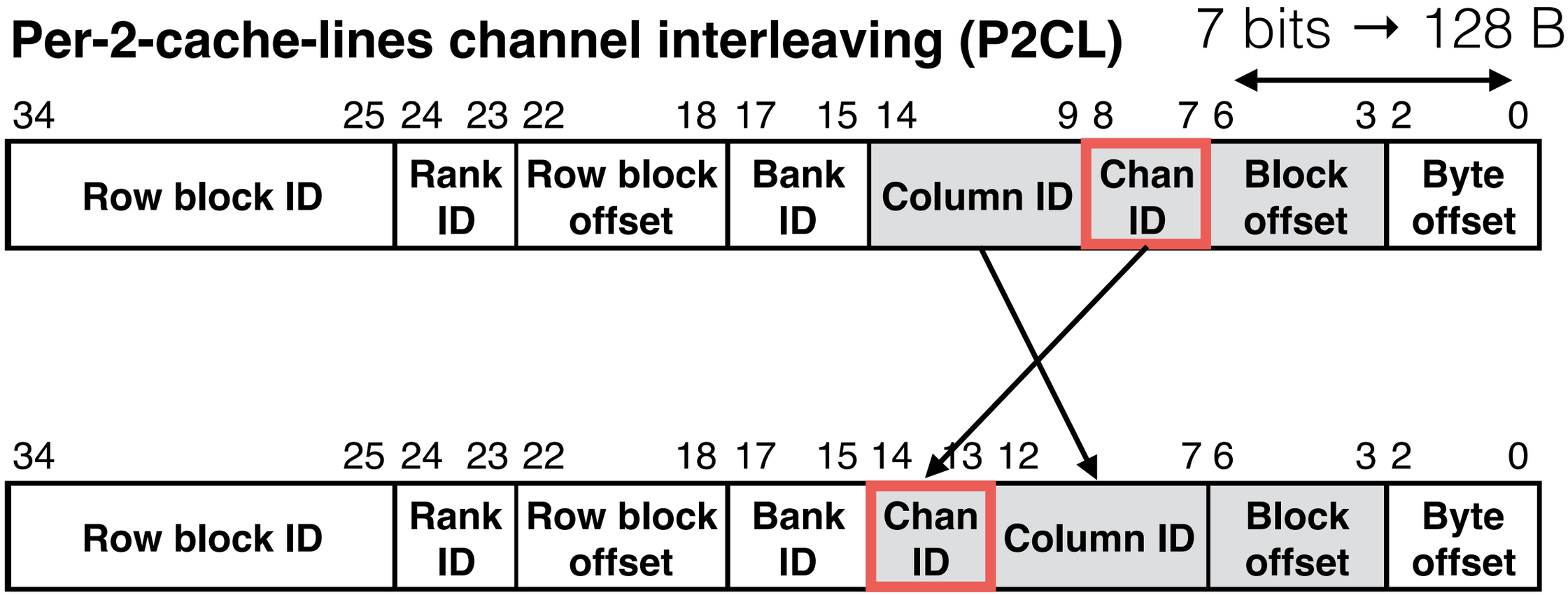

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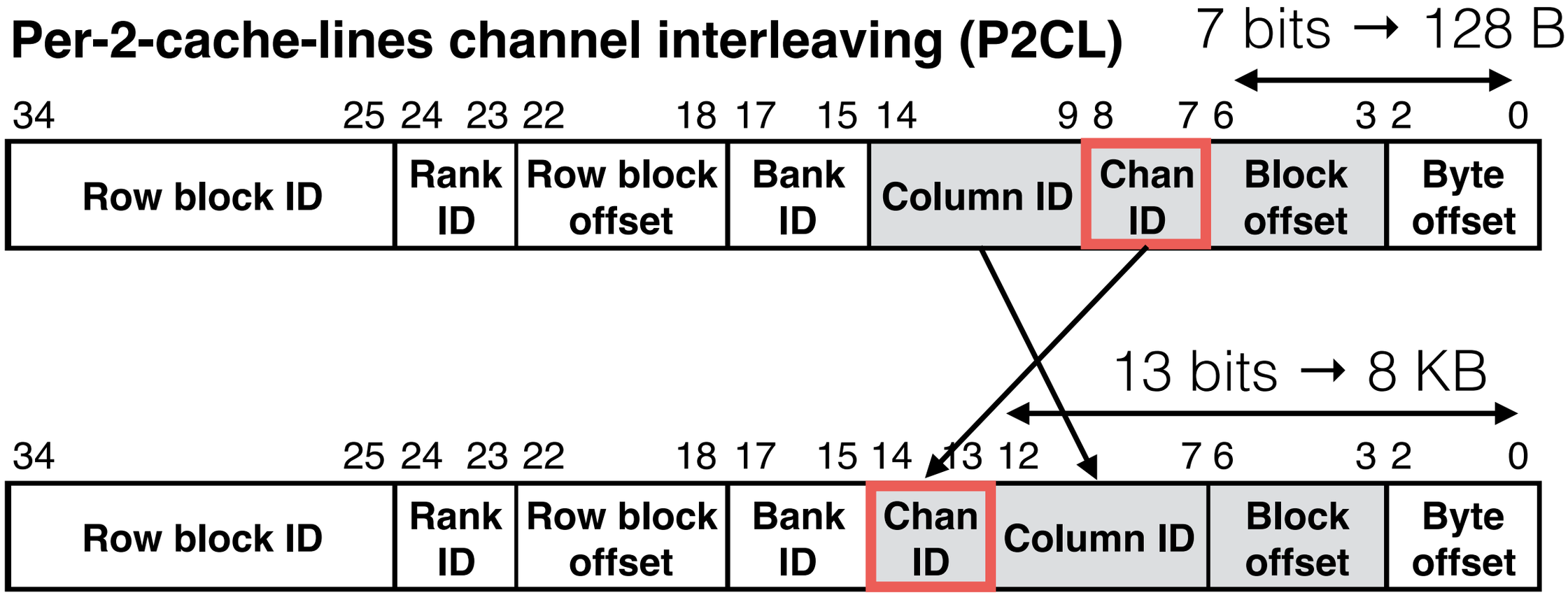
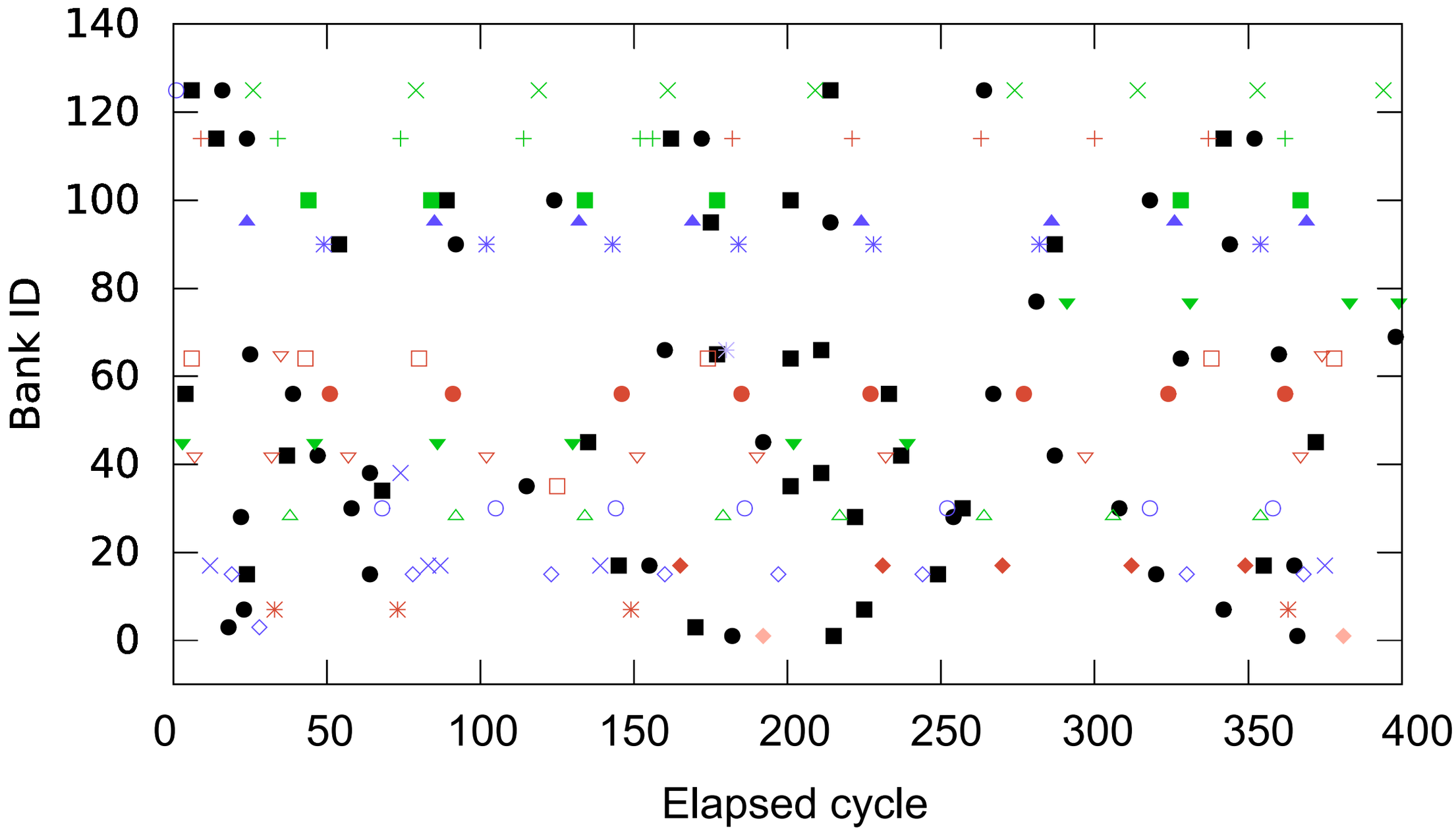


Memory Access Trace with PR



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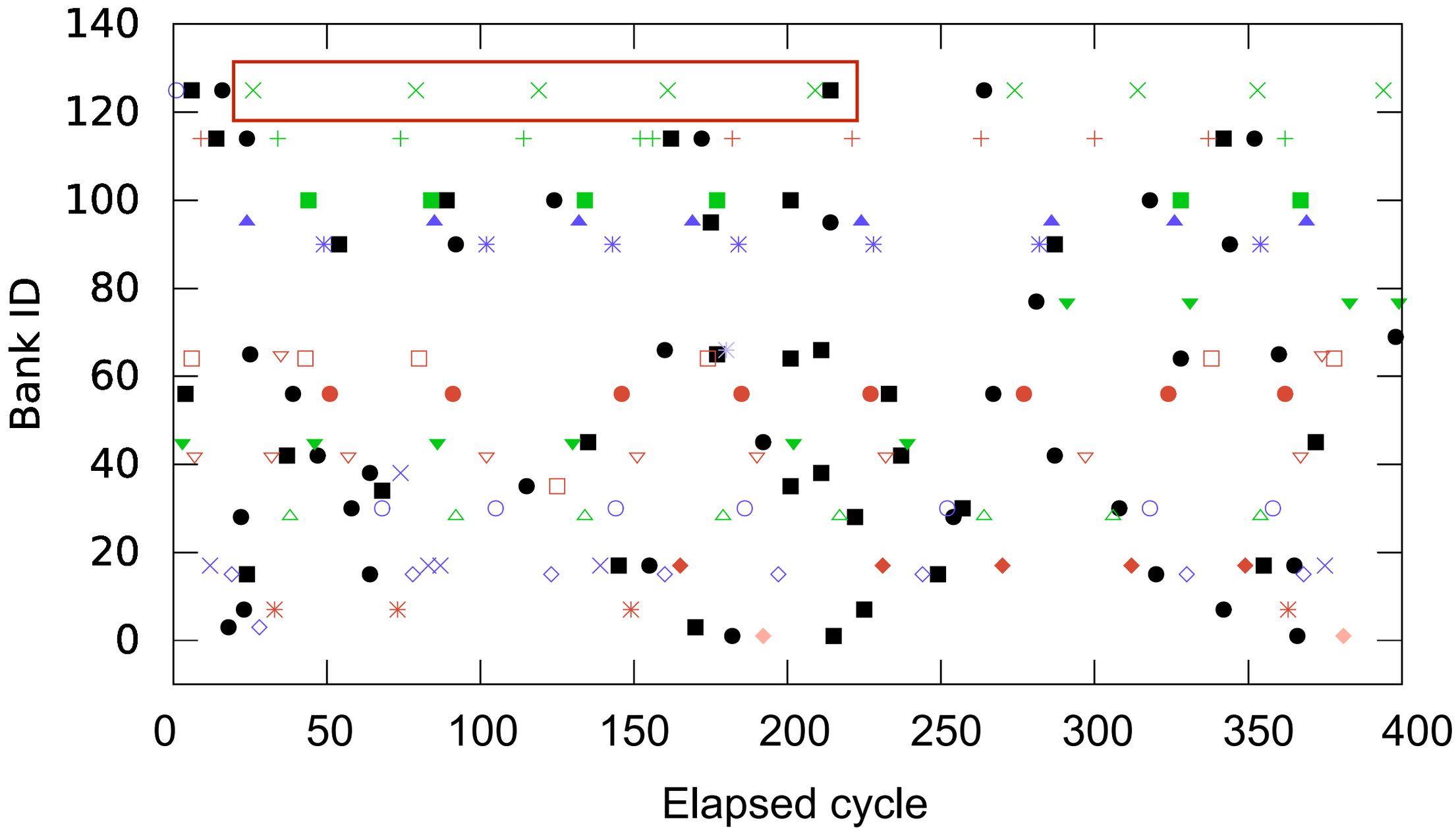

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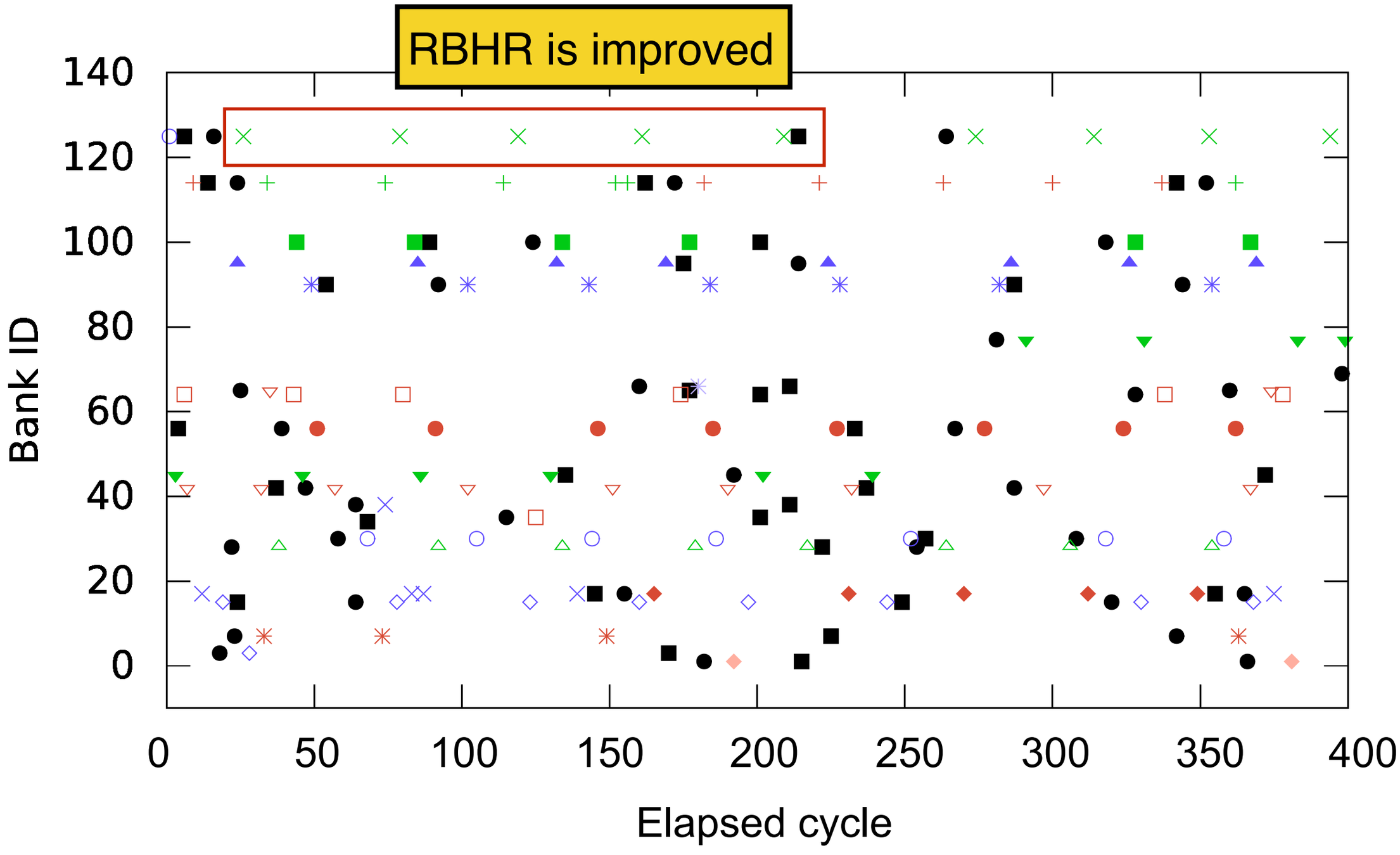

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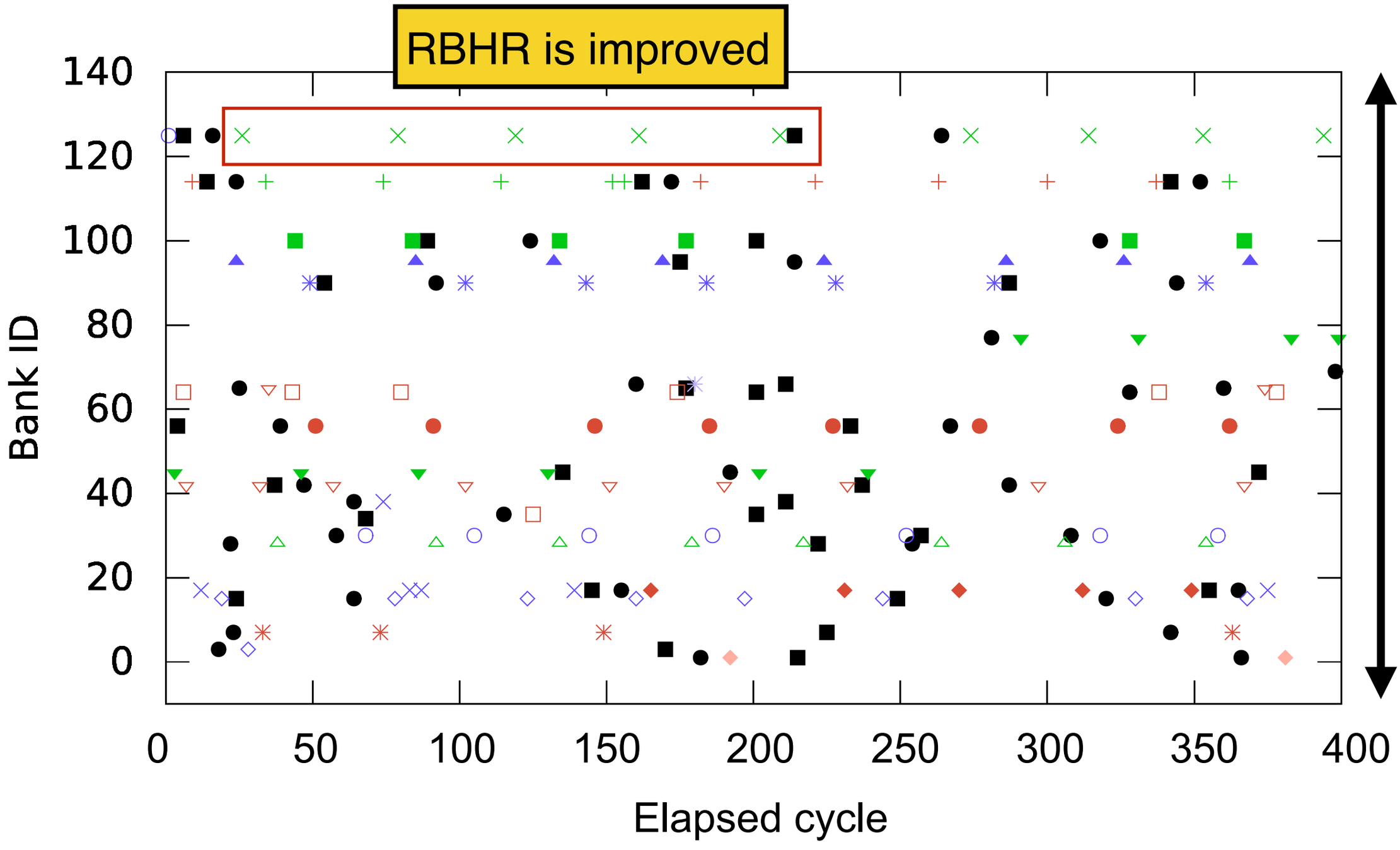

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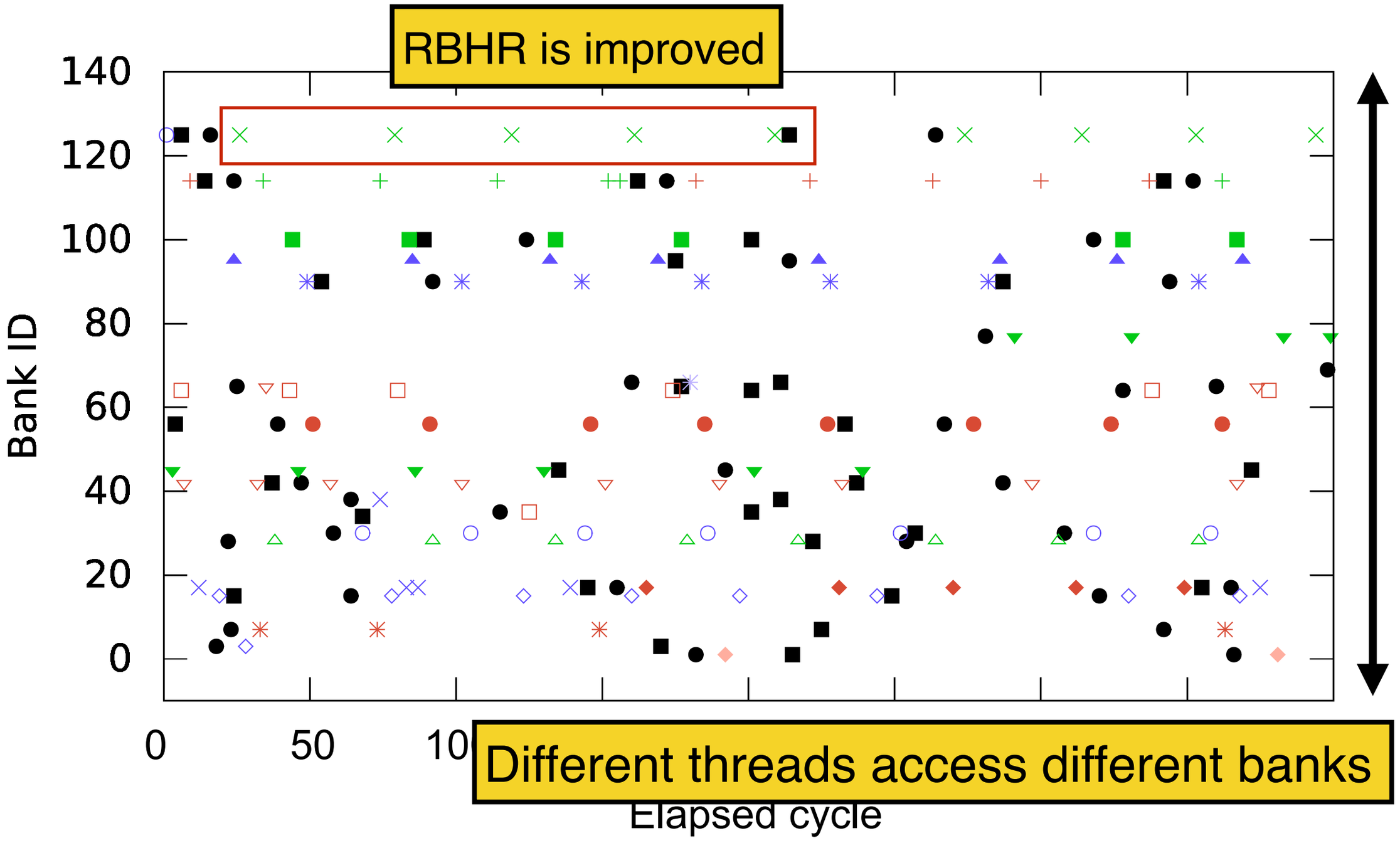

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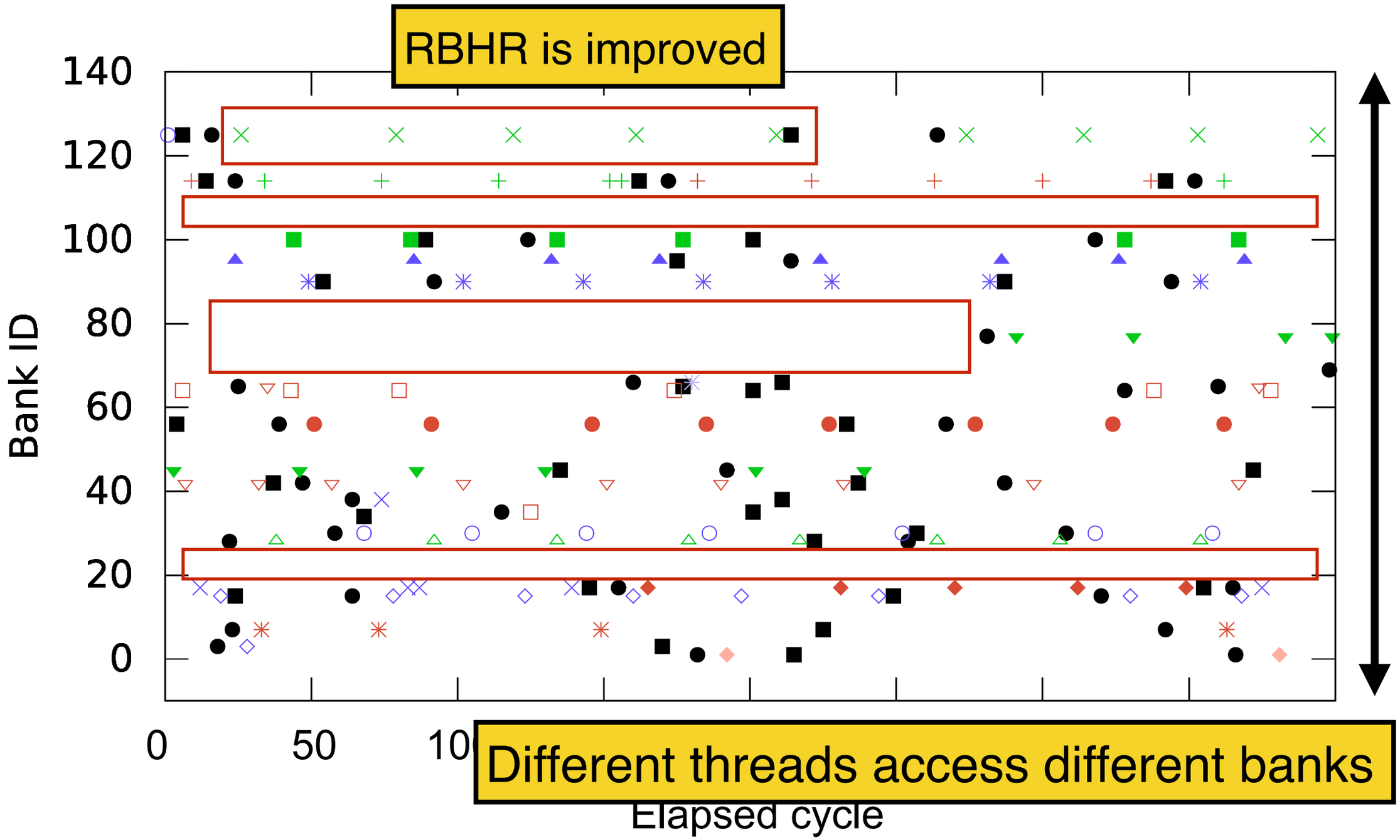

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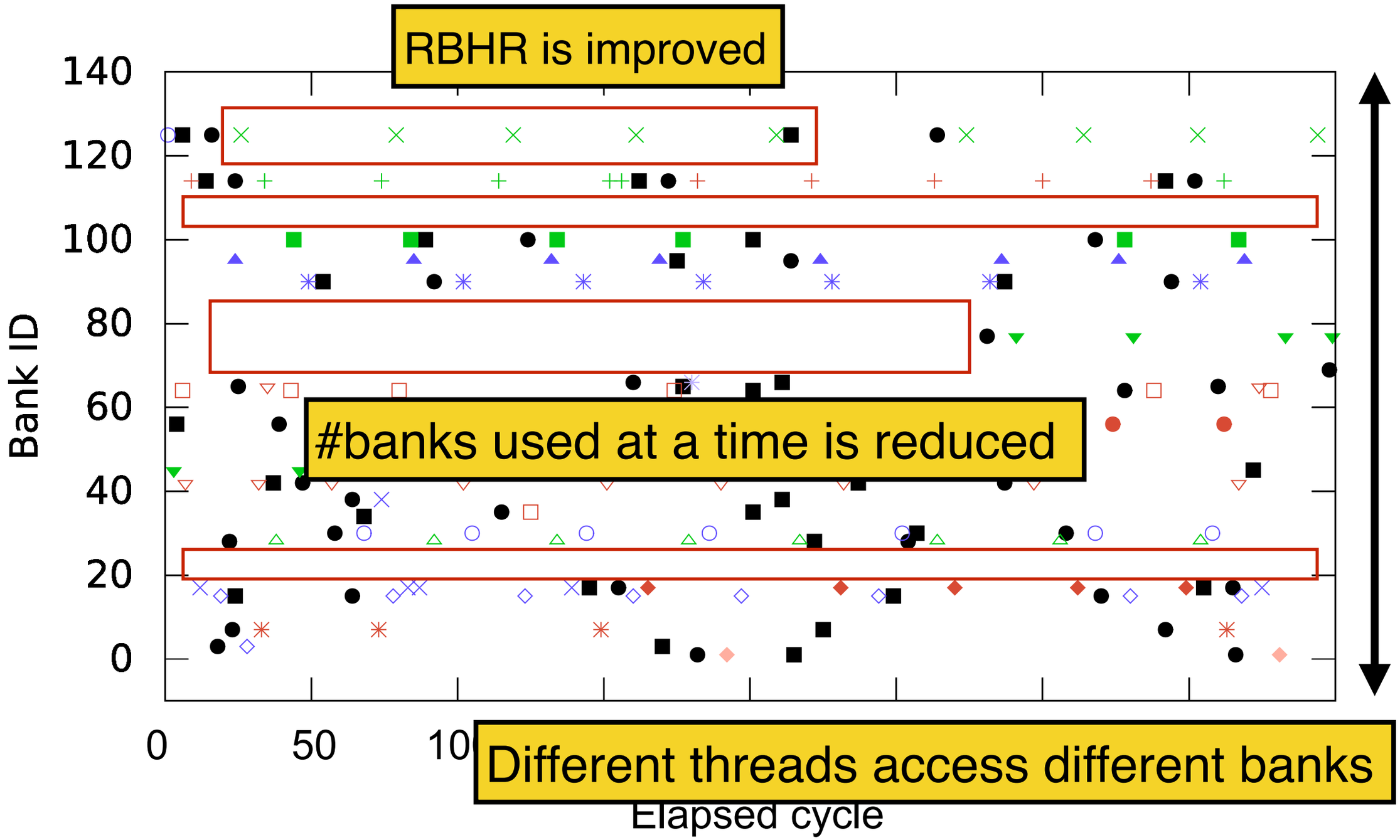
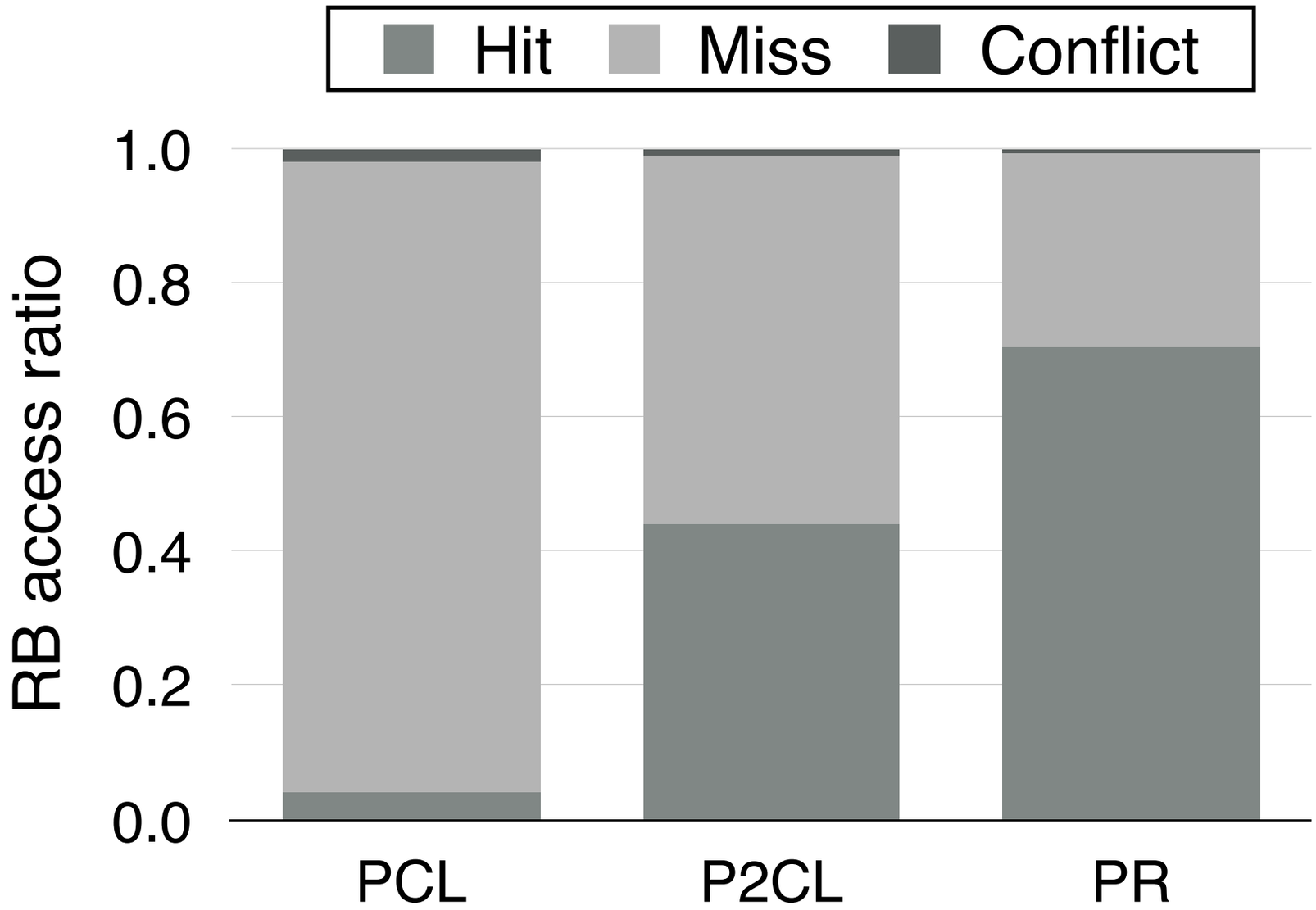


Agenda

- Graph analysis applications and Graph500
- State-of-the-art Graph500 implementation
- DRAM mechanisms
- Memory access analysis with conventional address mapping schemes
- Proposed: per-row channel interleaving
- Evaluation of power efficiency

Row Buffer Access Ratio



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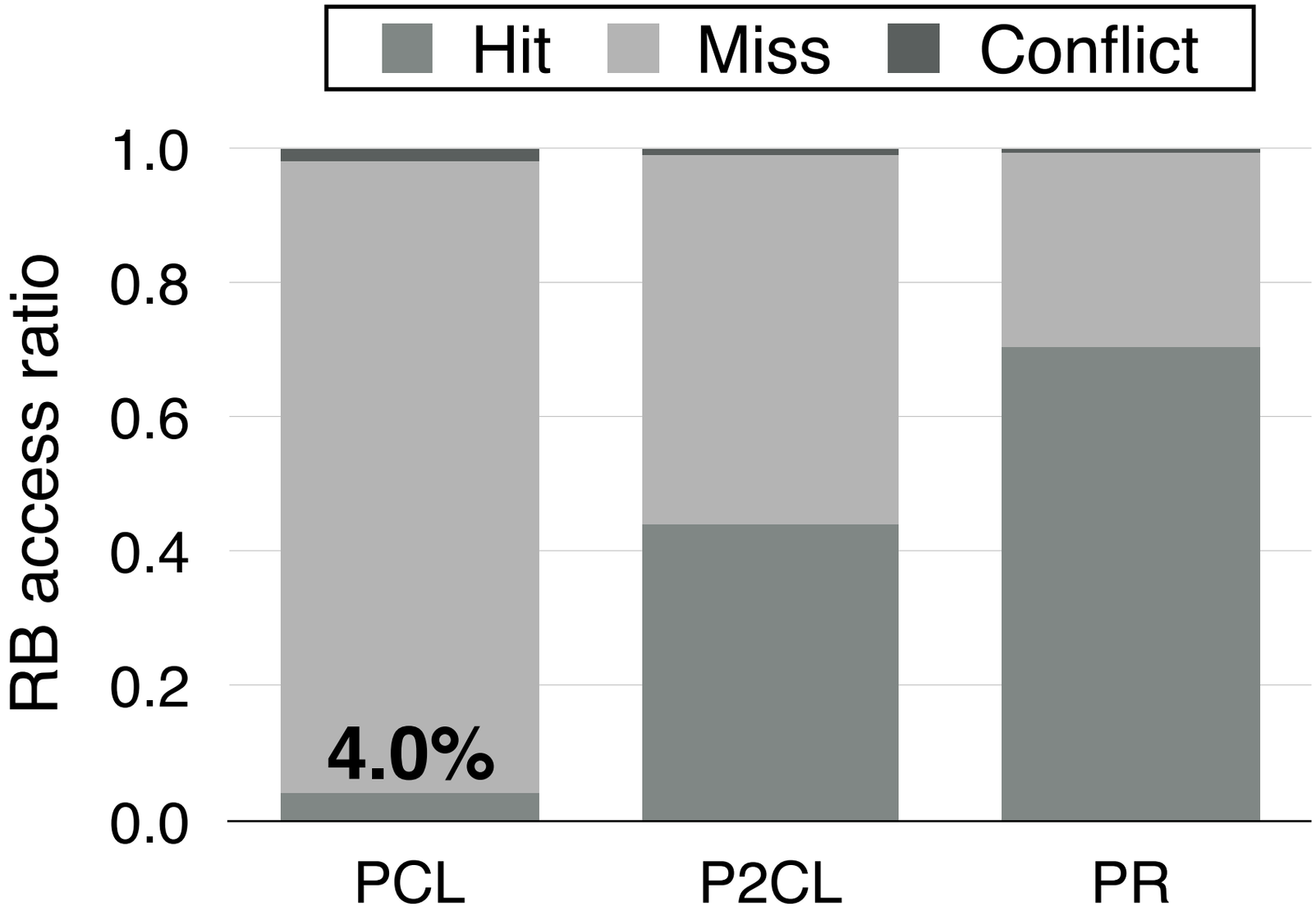

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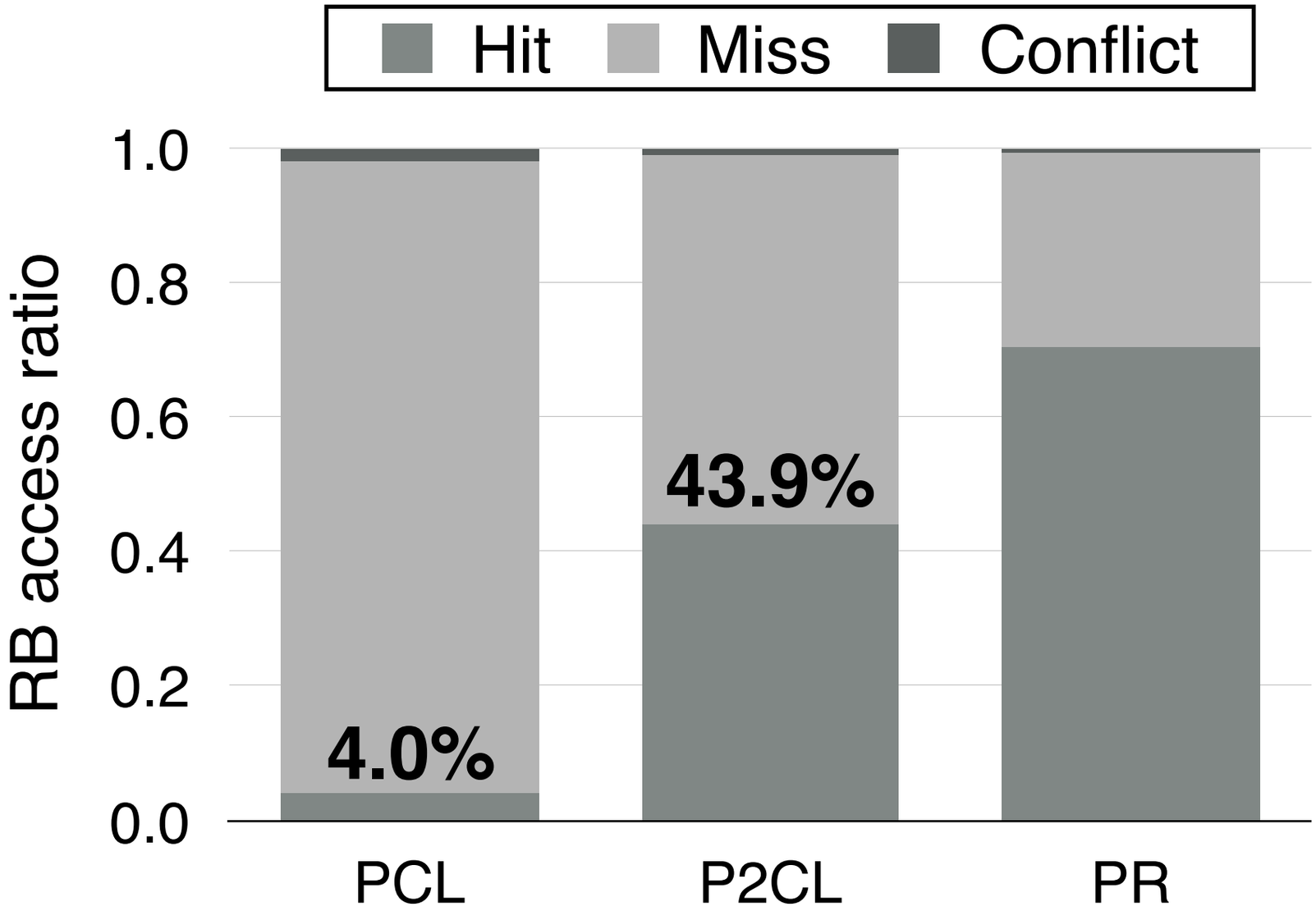

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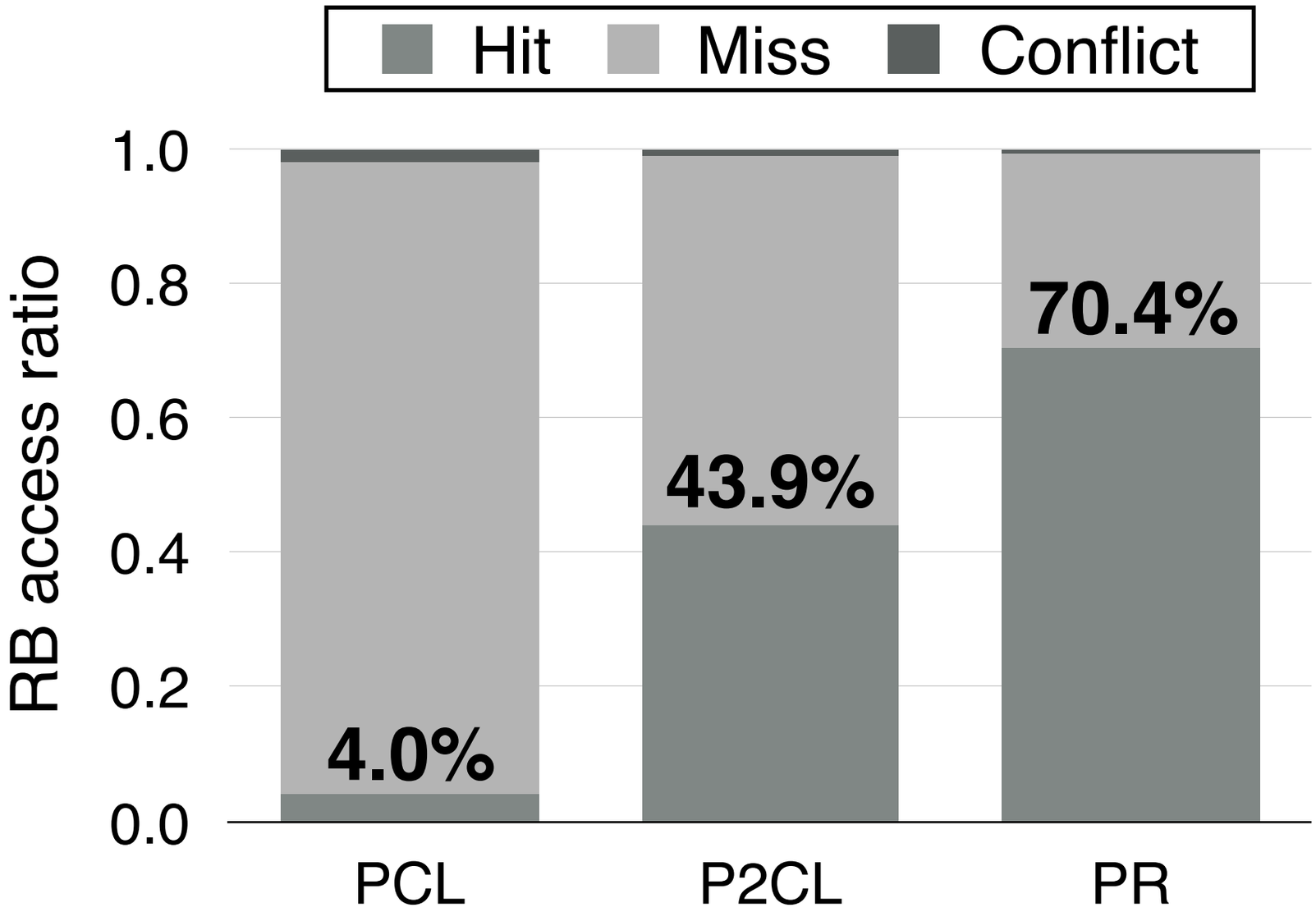
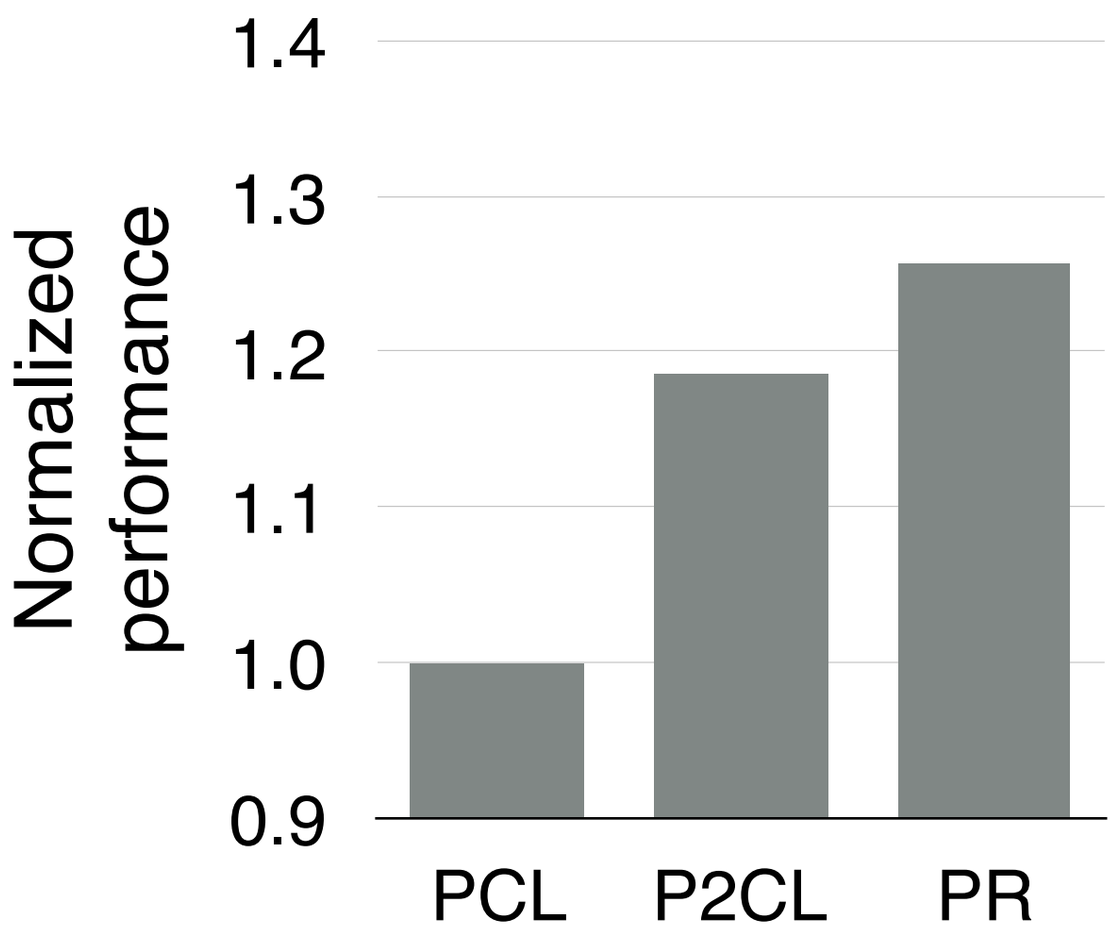


Performance & Power



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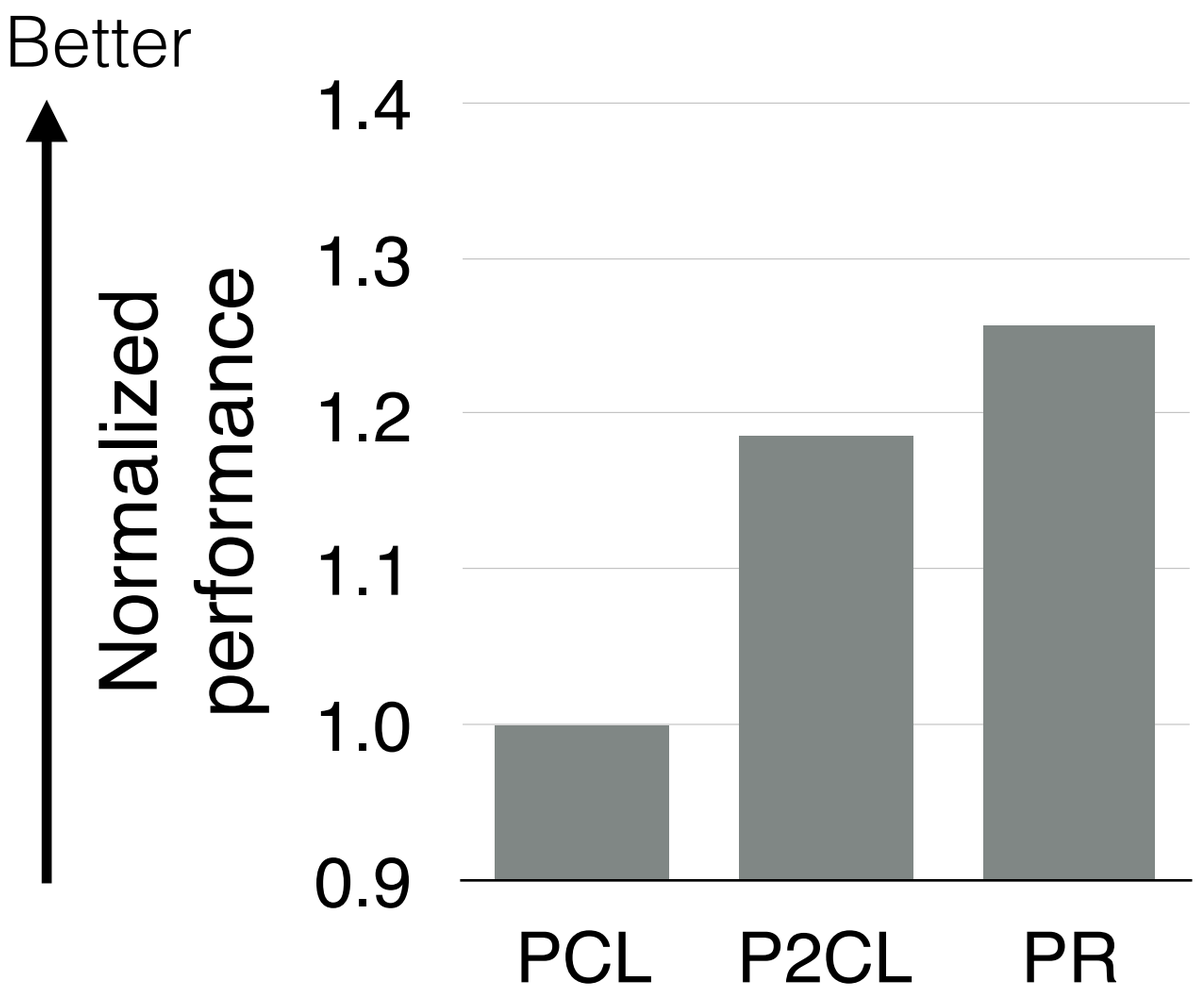

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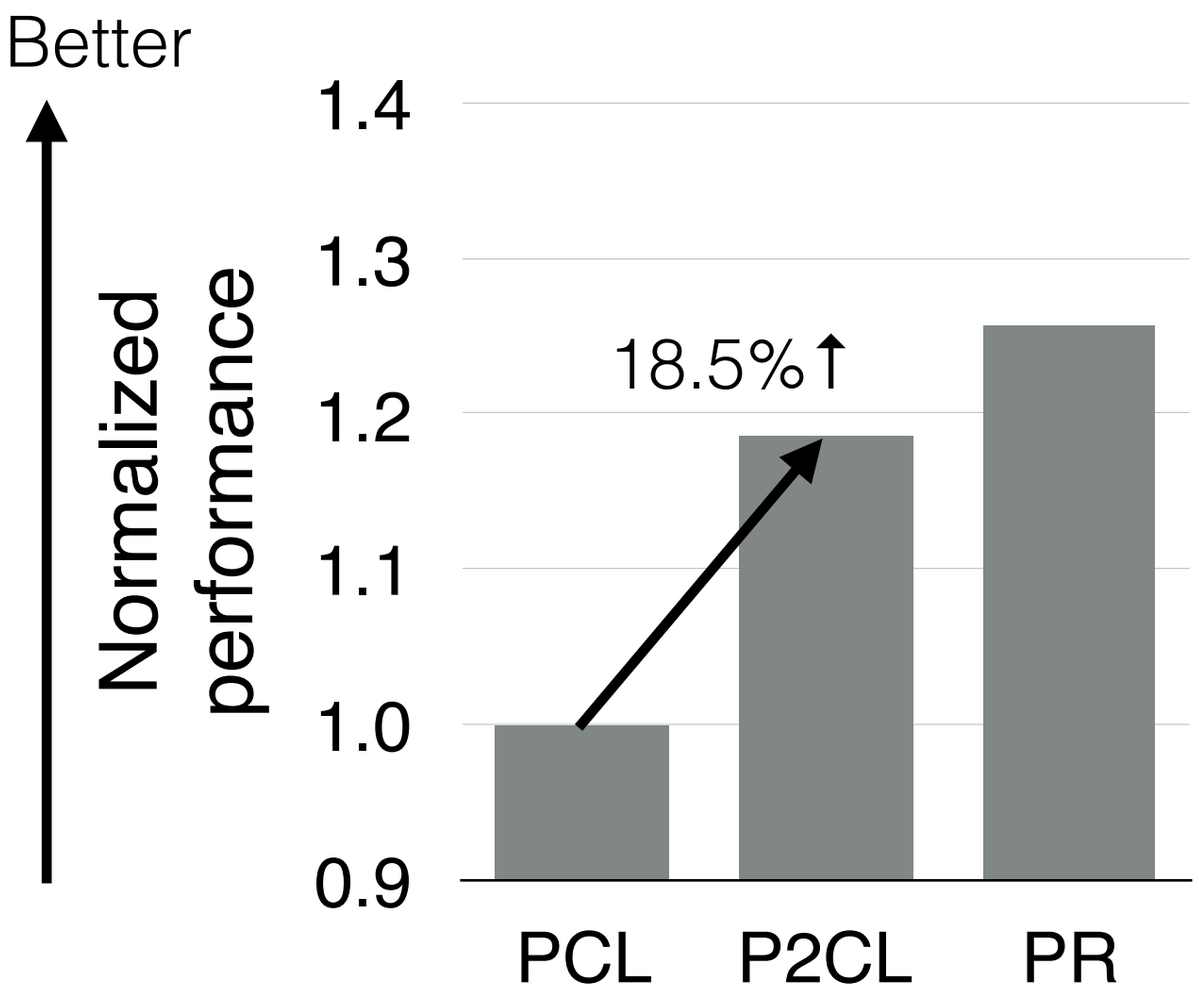

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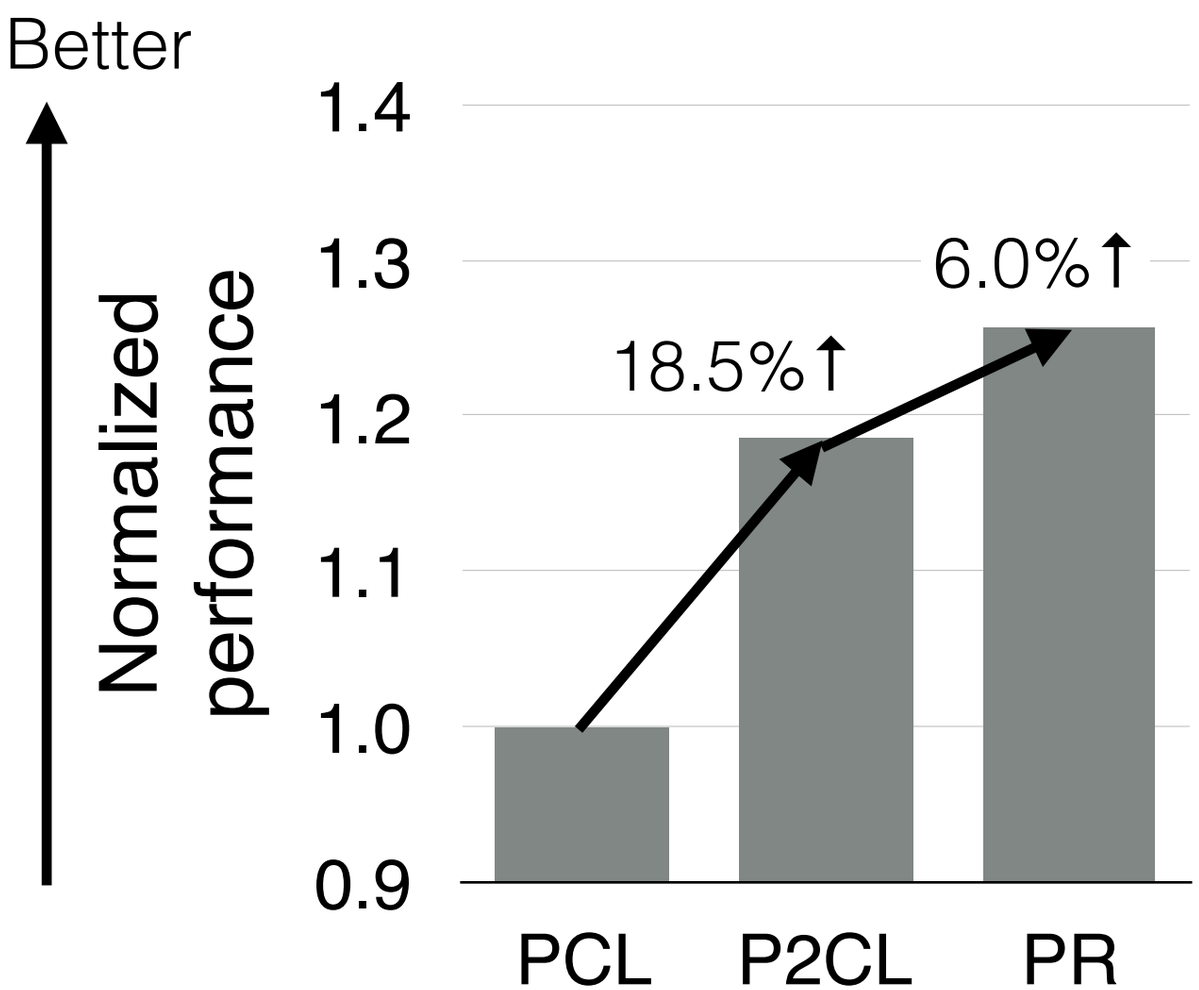

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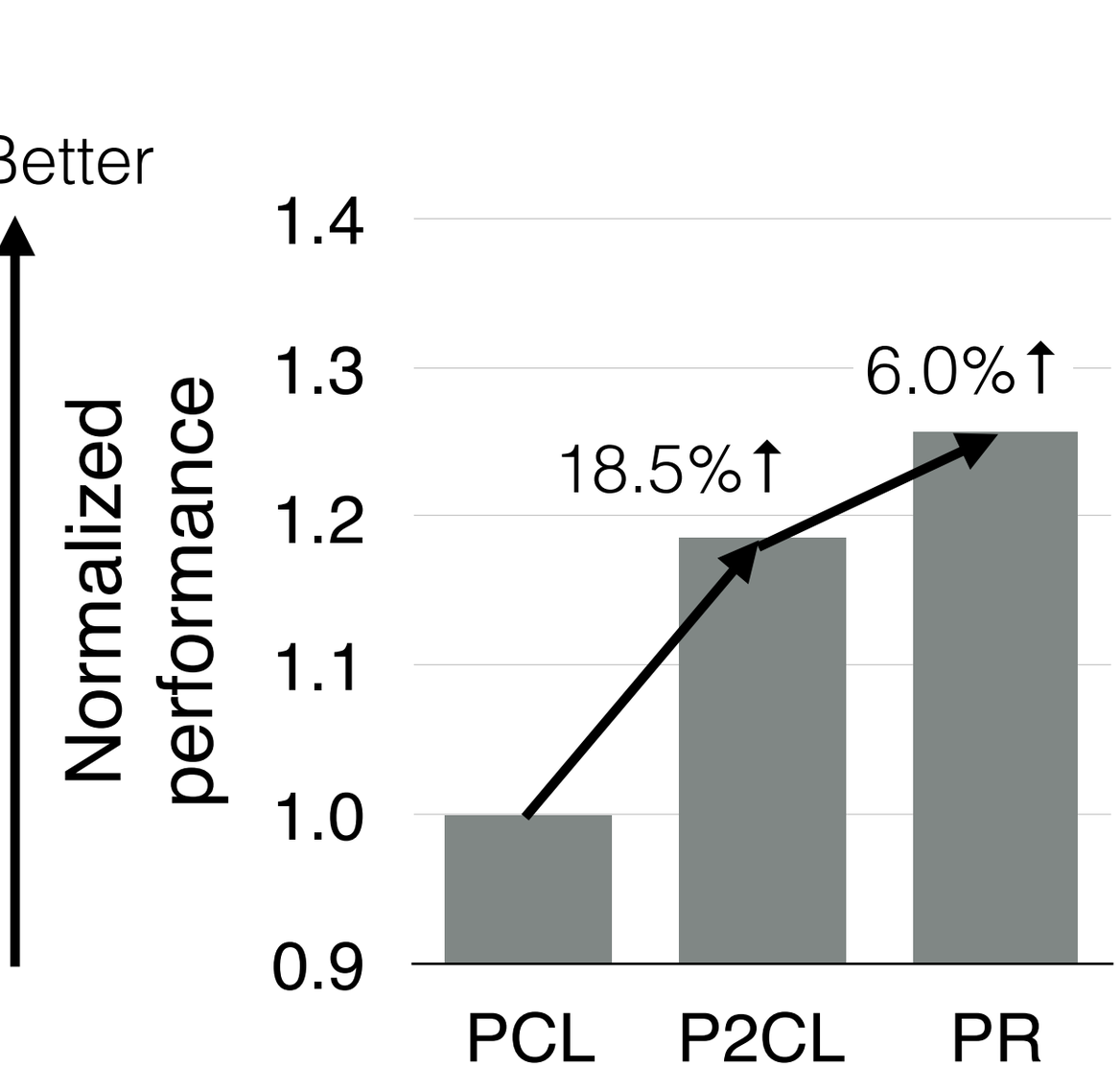

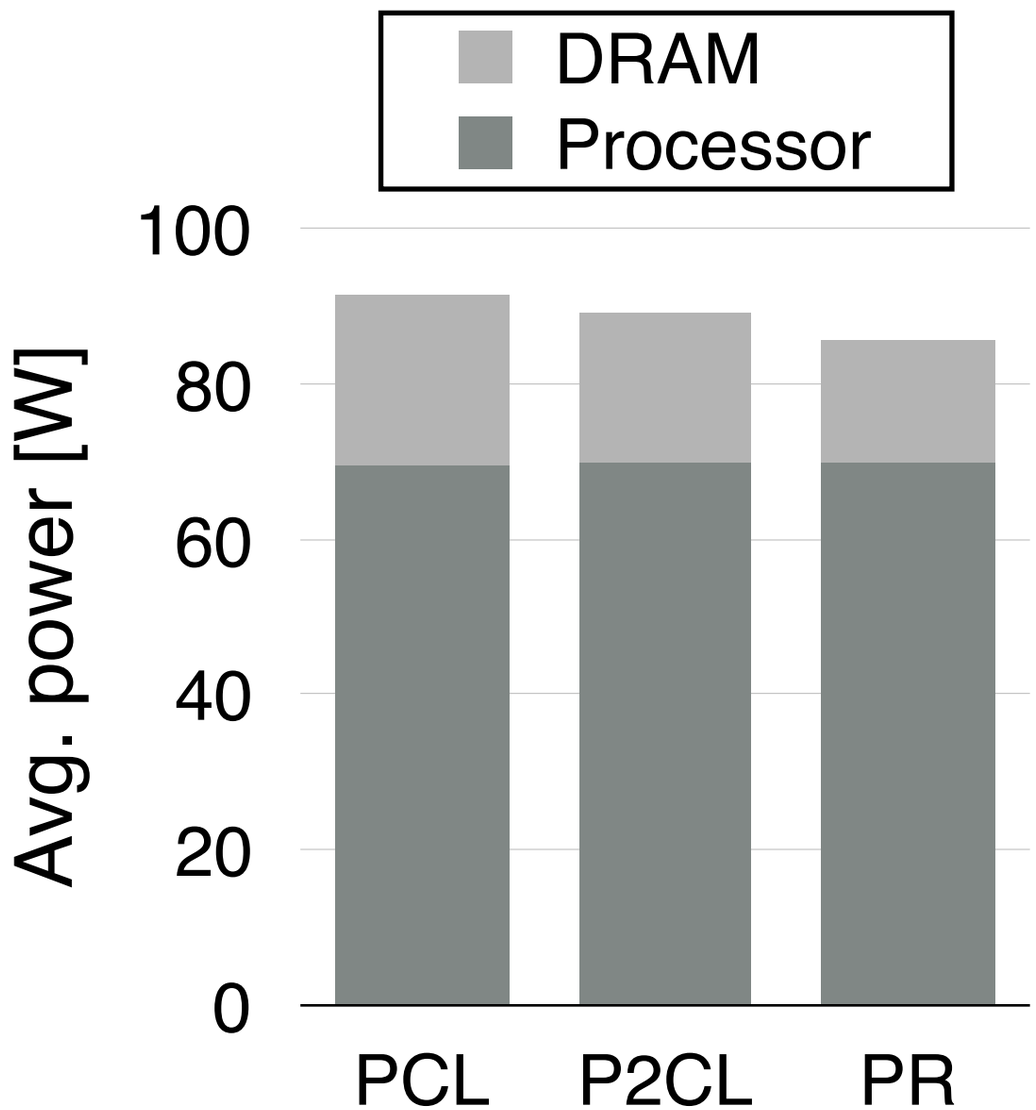

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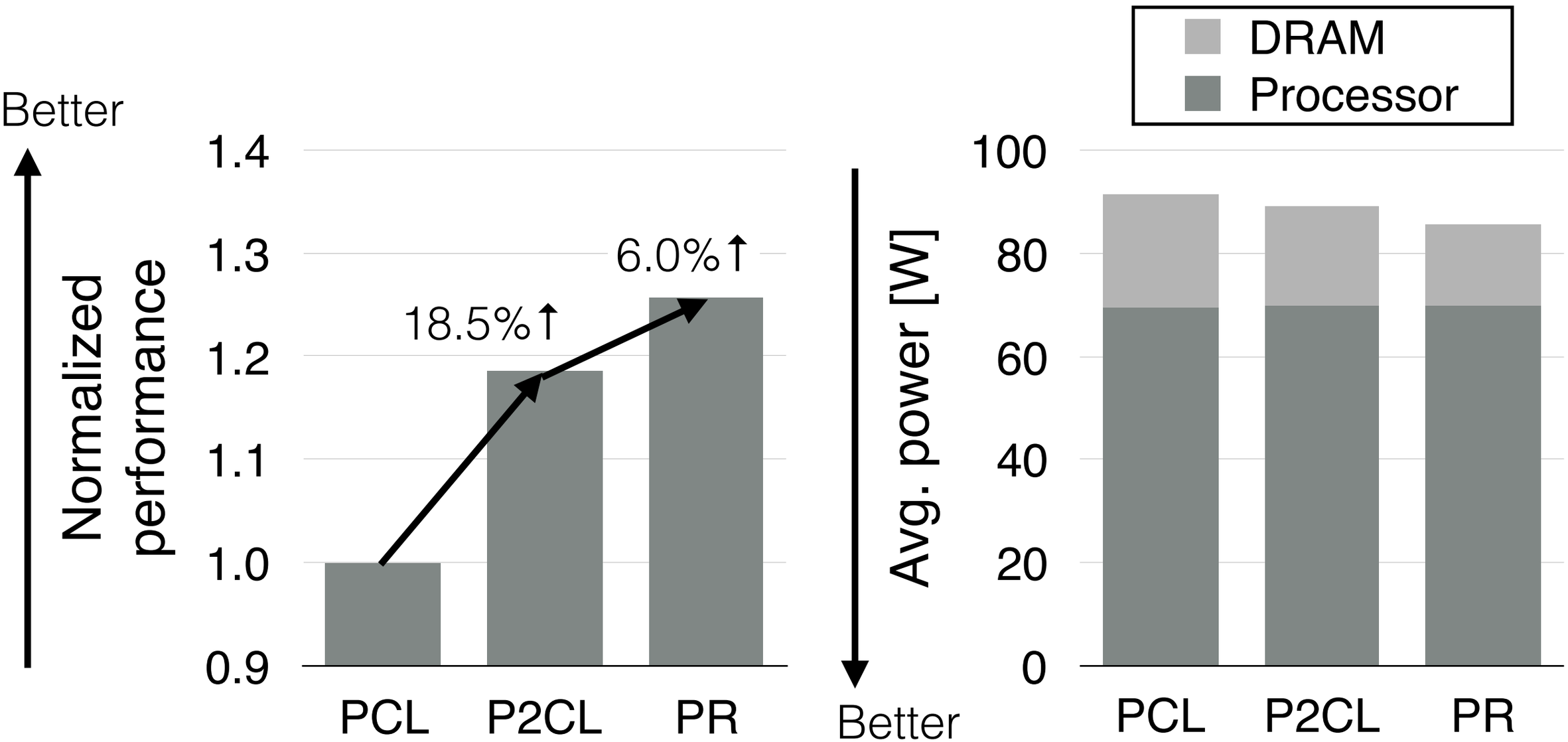

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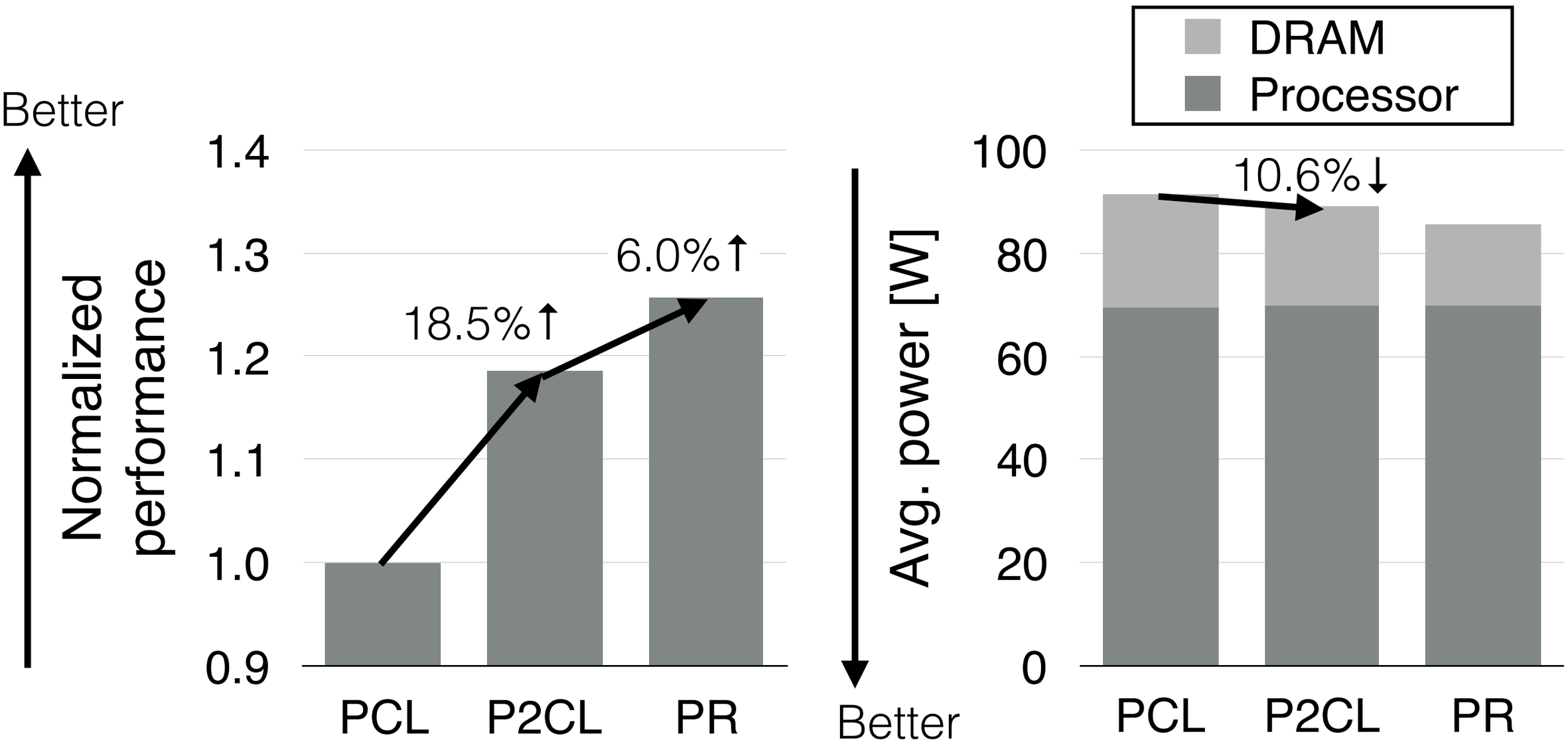

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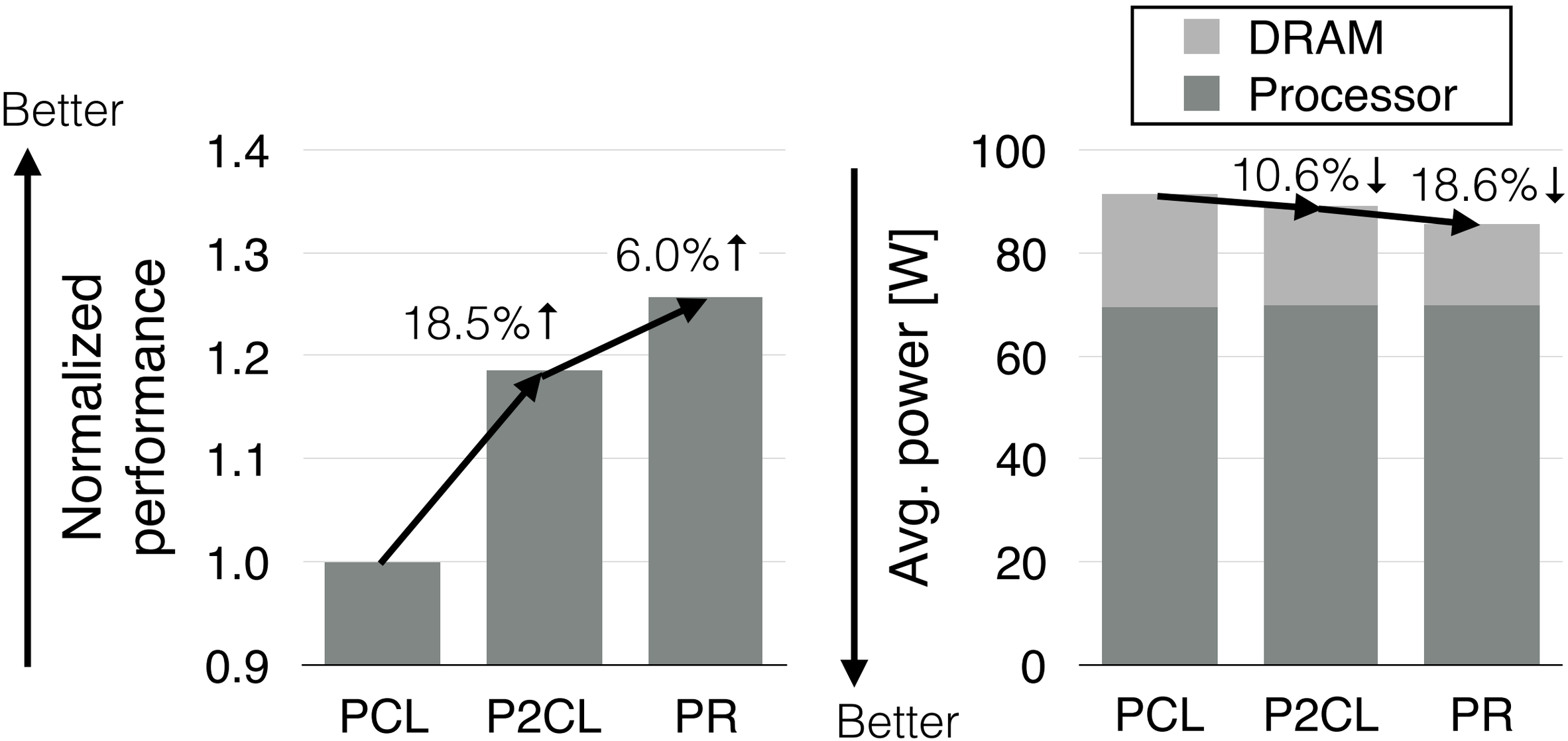
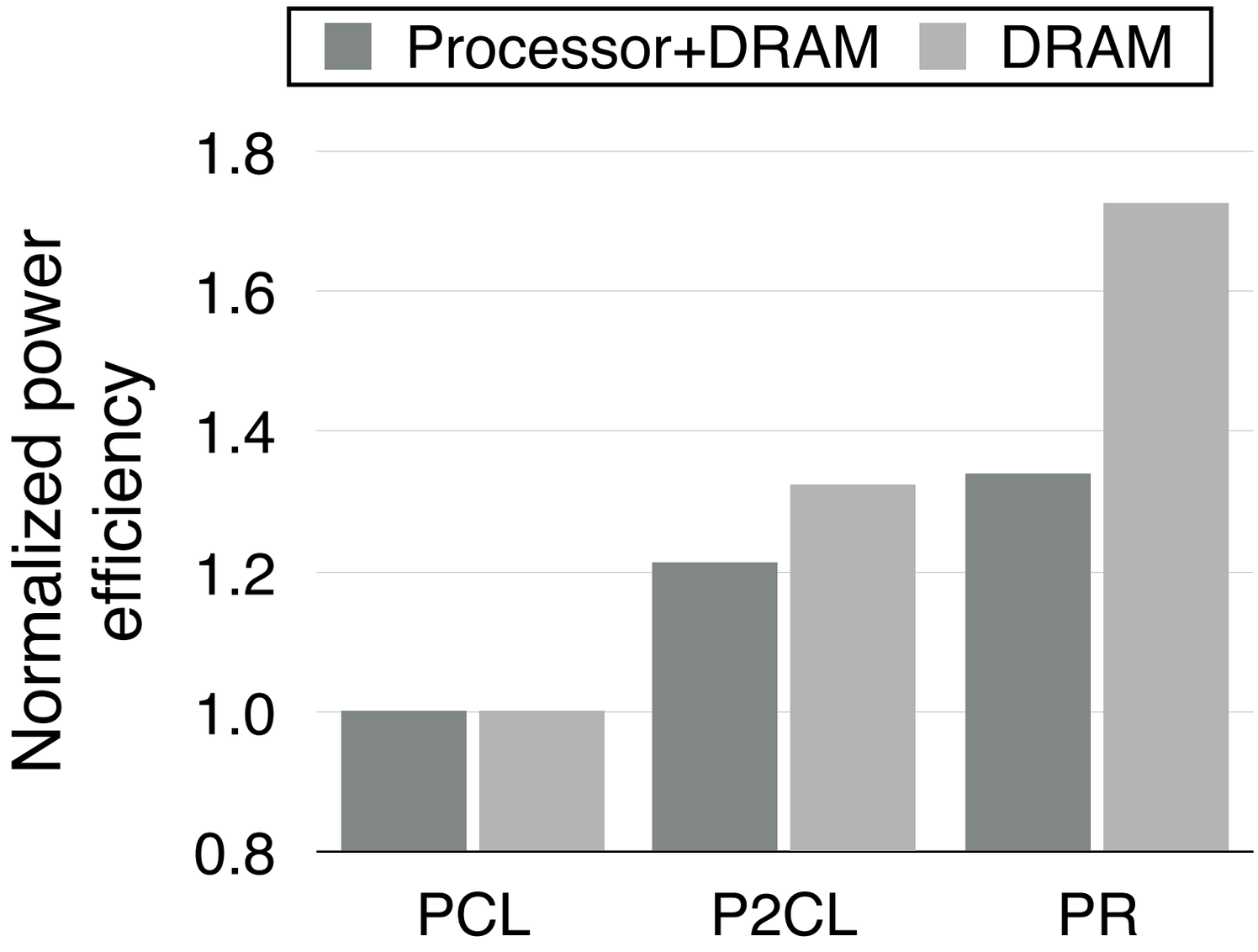


Power Efficiency



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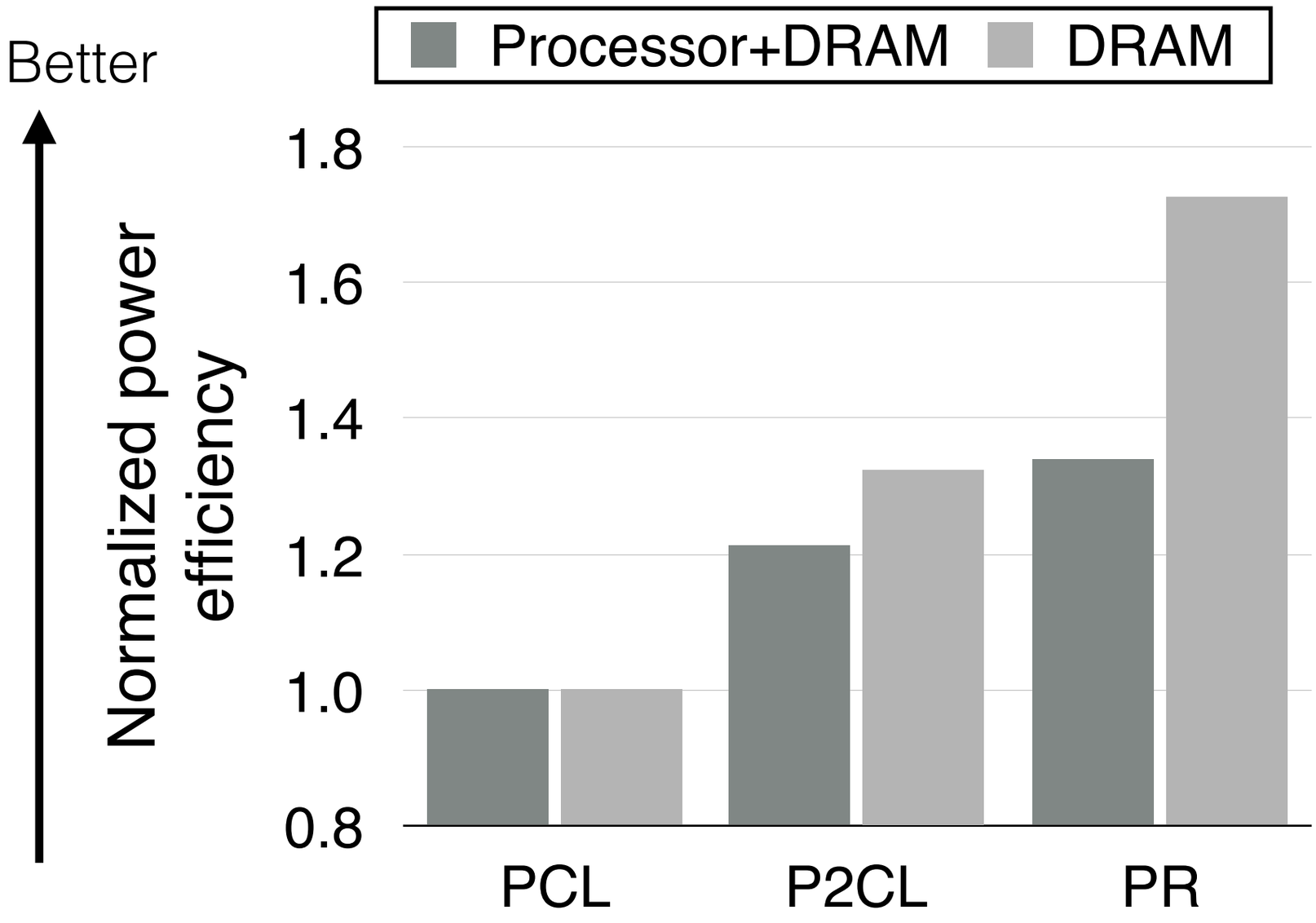

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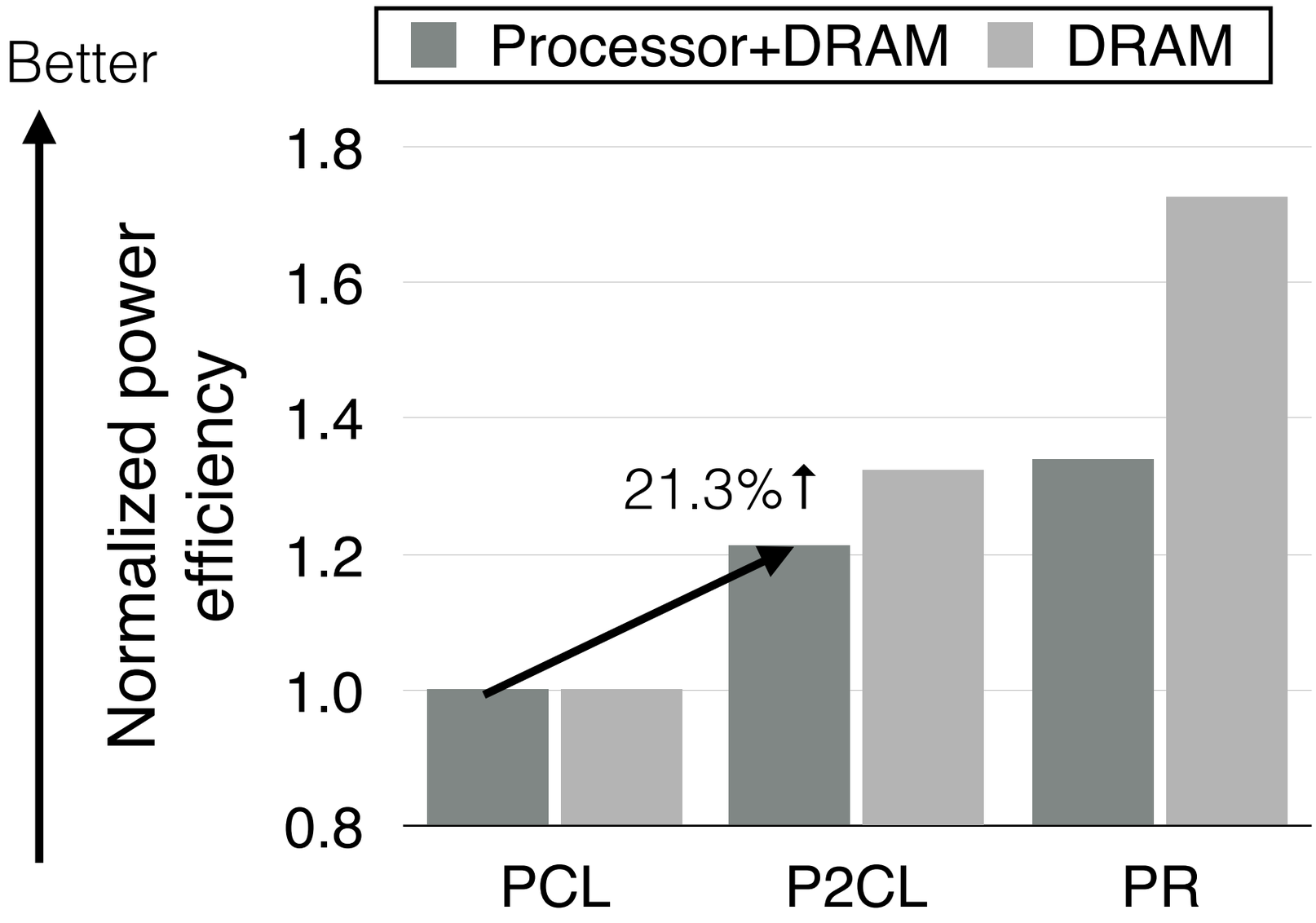

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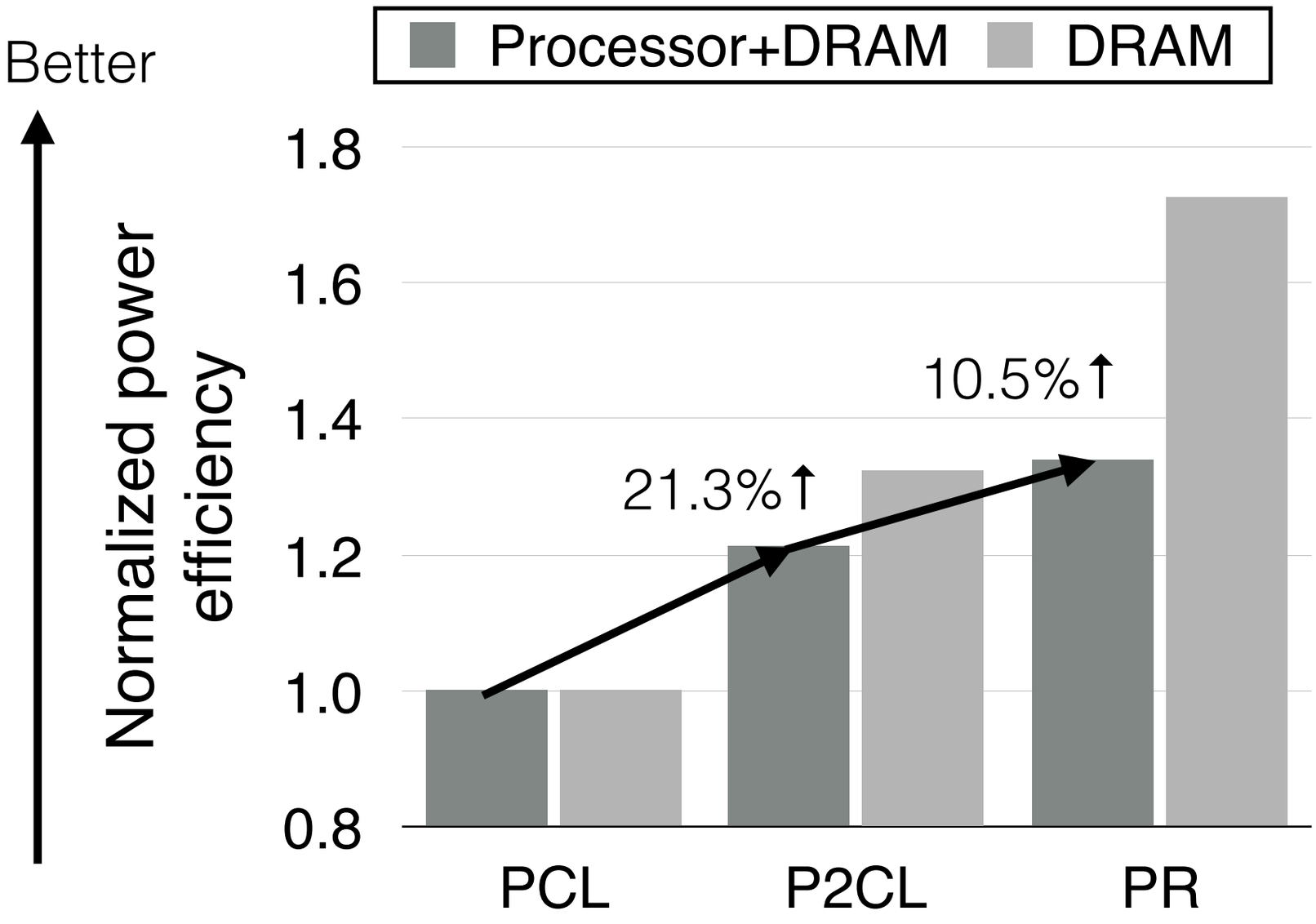
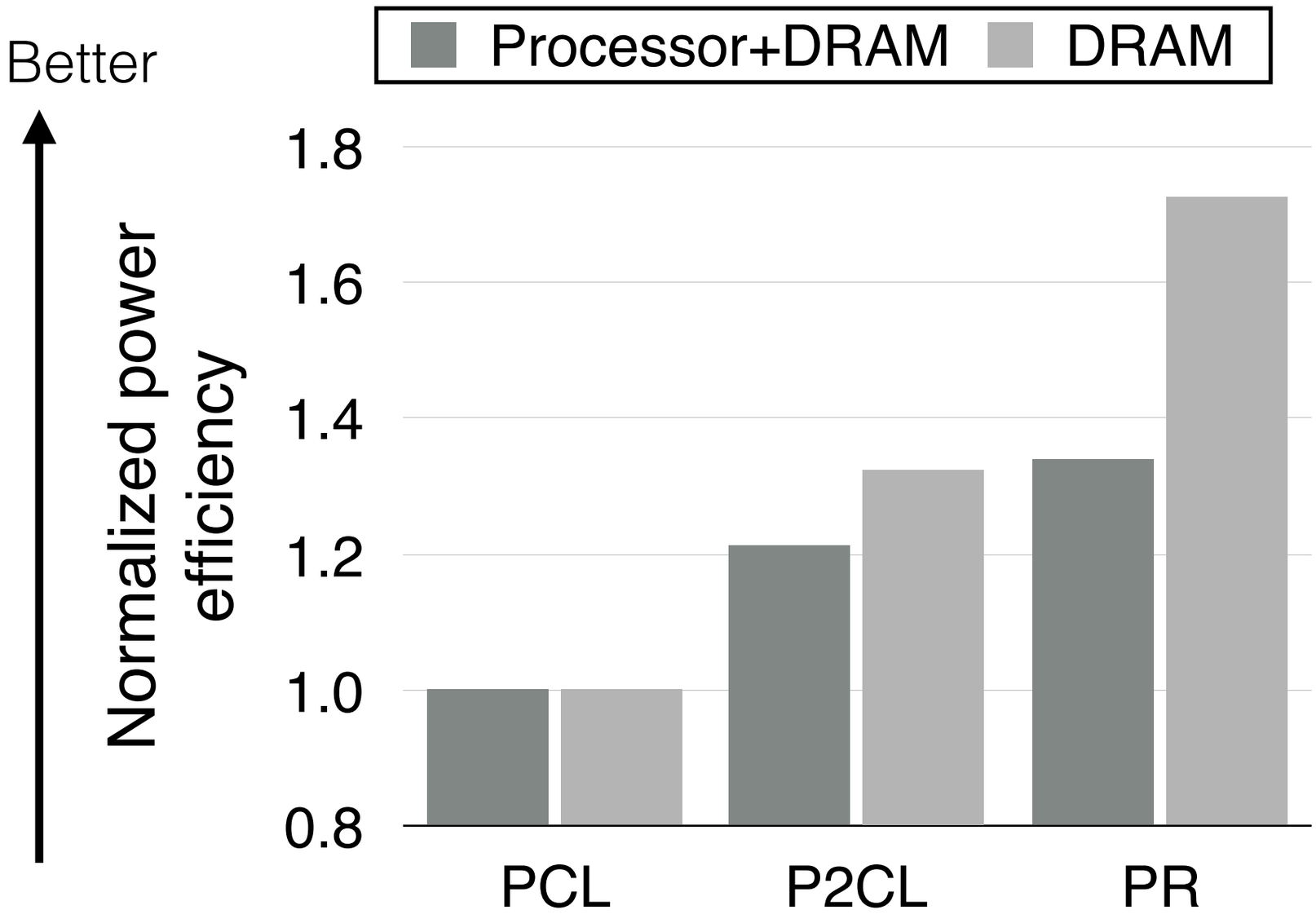
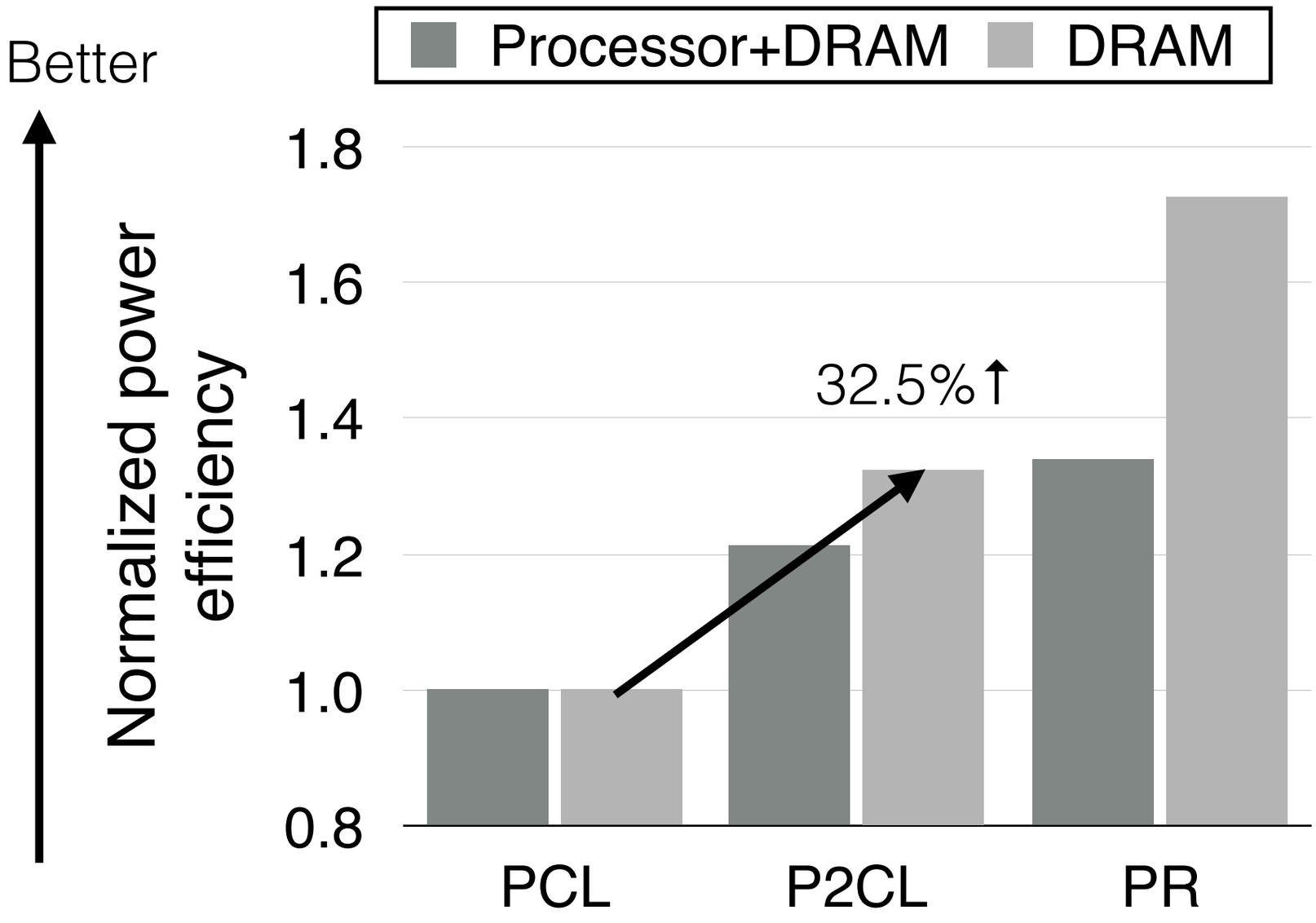


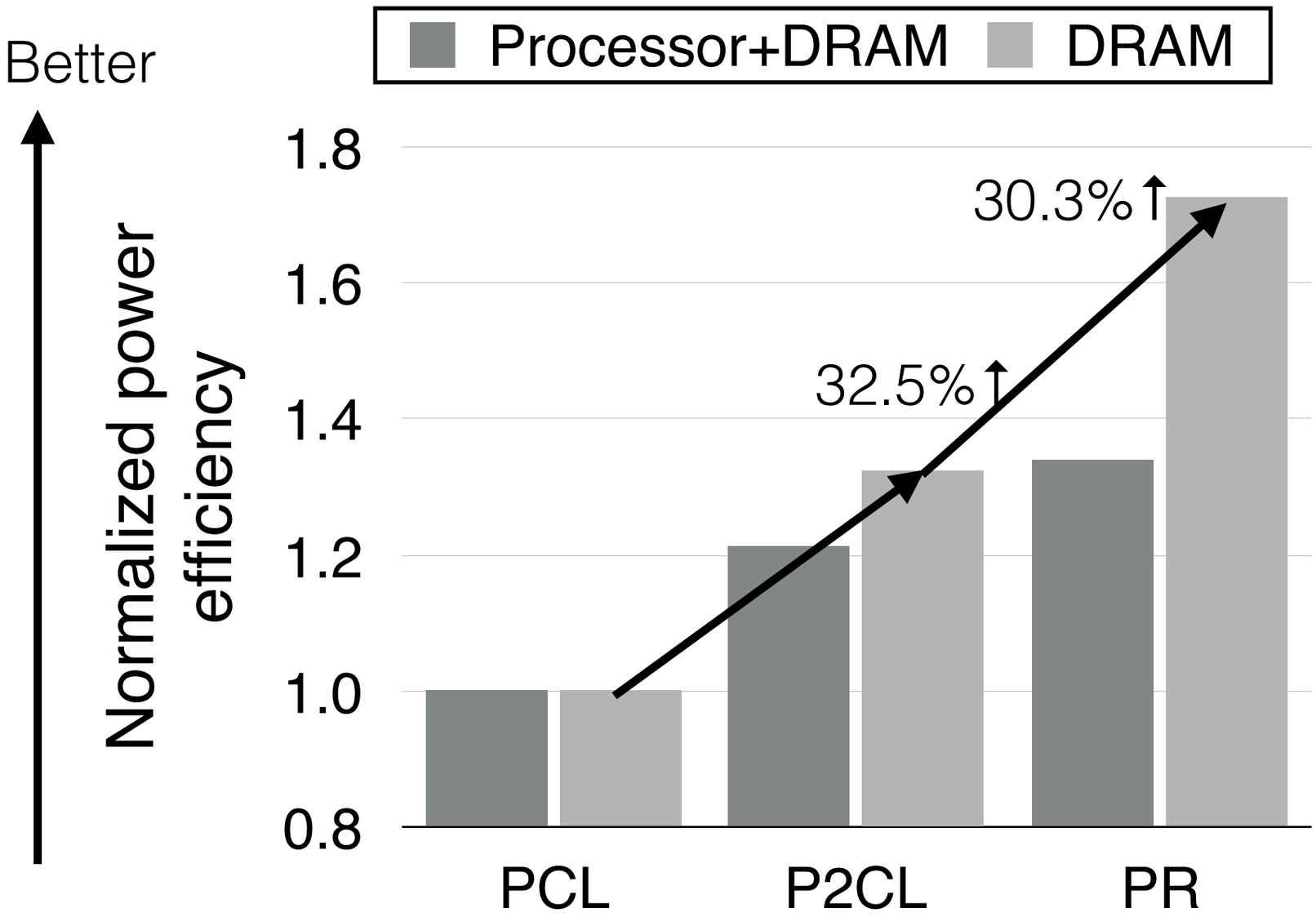
Power Efficiency



Power Efficiency



Power Efficiency



Conclusions

- It is a big challenge to improve the power efficiency of BFS
- Conventional address mapping schemes do not efficiently utilize DRAM in bottom-up algorithm
- We propose per-row channel interleaving
  - It improves RBHR and DRAM power efficiency by 30.3%
- Future work
  - Evaluate PR with other graphs/algorithms/applications with various memory access patterns

Power-Efficient Breadth-First Search with DRAM Row Buffer Locality-Aware Address Mapping

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